Engineered SOI substrates for RF applications

- current success and future perspective -

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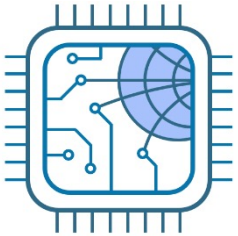
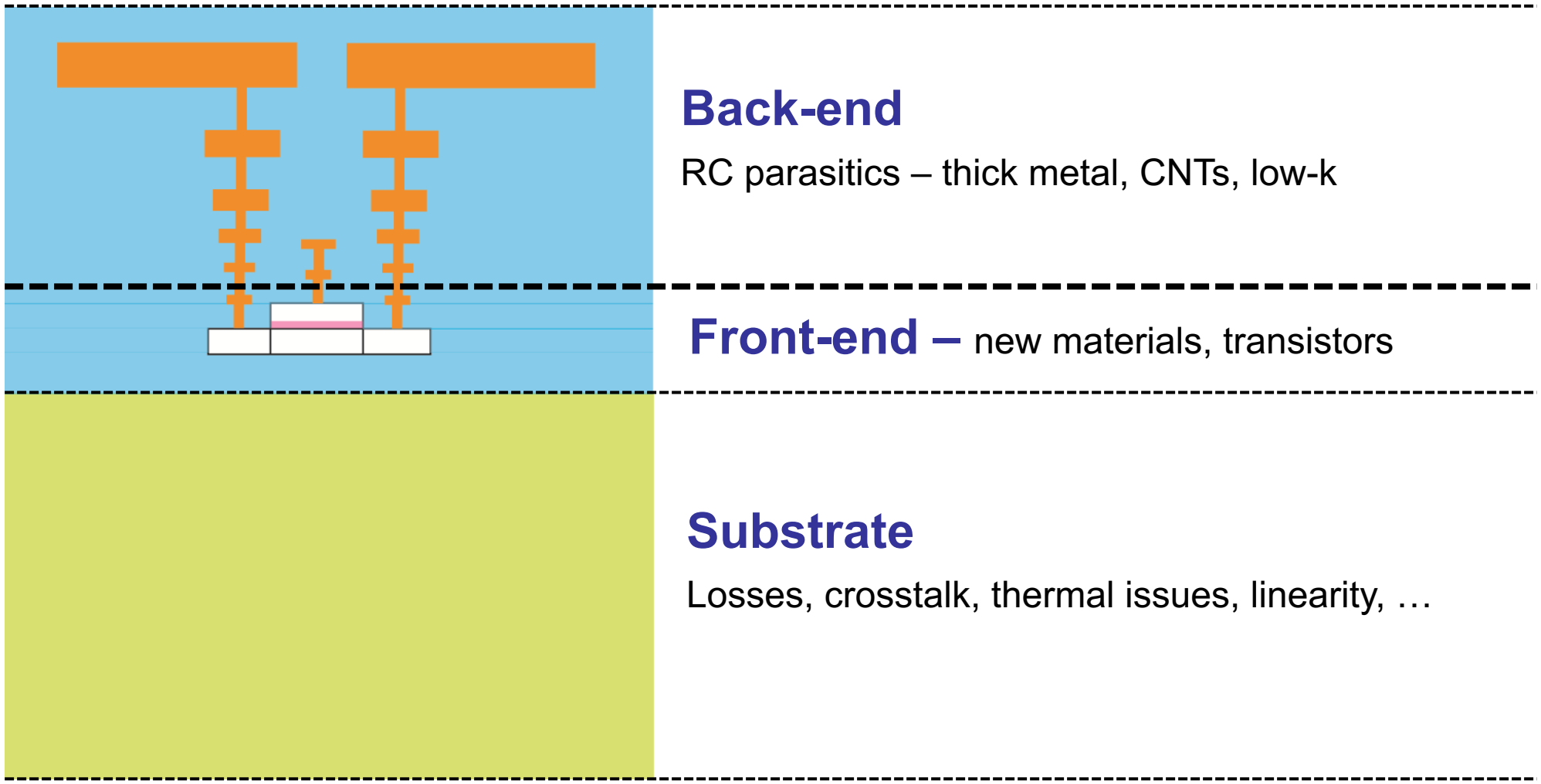


The 10th anniversary of Incize, Castle Terblock, Overijse, Belgium, 2024

Nanoelectronics – challenges at different levels …



Back-end

RC parasitics – thick metal, CNTs, low-k

Front-end – new materials, transistors

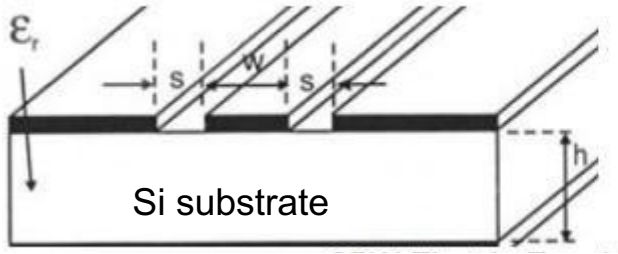
Substrate

Losses, crosstalk, thermal issues, linearity, …

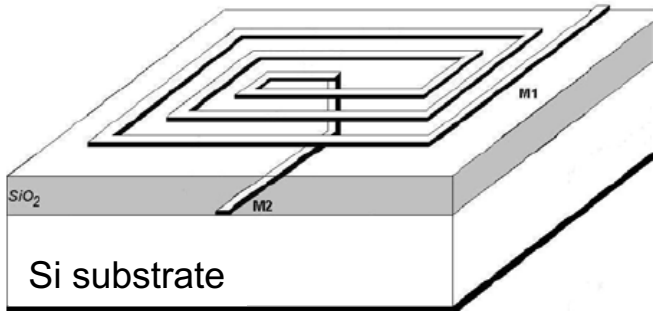
[J.-P. Raskin, *Solid-State Electronics*, 2016]

Need for high resistivity Si substrate

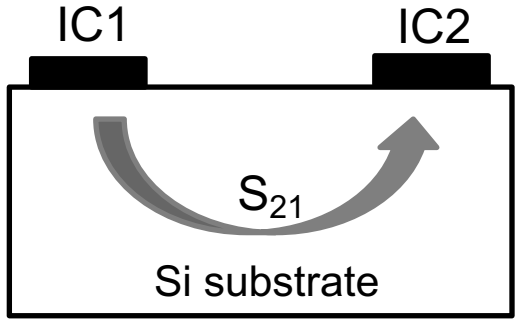
Transmission line

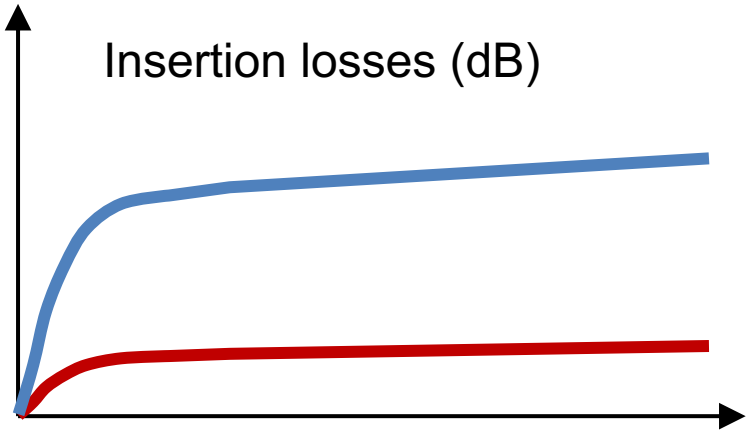


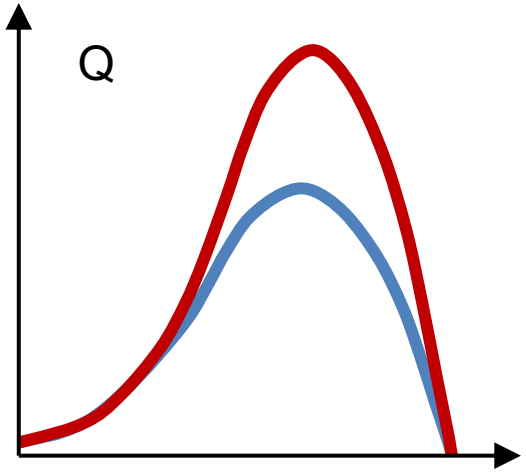
Inductor

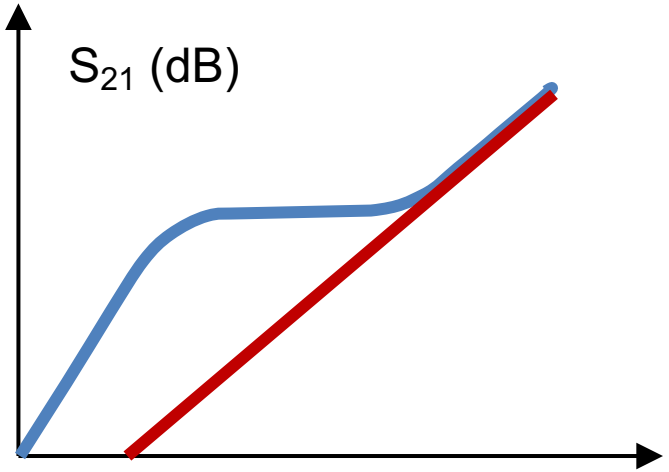


System-on-Chip









Standard resistivity (10 Ω.cm)

High resistivity (10 kΩ.cm)

RF-SOI substrates: State-of-the-Art

100 mm

300 mm

Wafer scale up

1992	1997	2005	2012	2019
SOITEC Smart Cut™	HR SOI (UCLouvain)	Trap-rich SOI (UCLouvain)	eSi substrate (SOITEC & UCLouvain)	Porous Si (Incize & UCLouvain)

Substrate effective resistivity increase

10 Ω.cm	0.1-1k Ω.cm	10 kΩ.cm	> 10 kΩ.cm

First steps towards RF-SOI

PhD thesis RF-SOI potentials

Technological solution for better substrates

Major industrial player asks for better, scalable and cheaper substrates

Mass market products

All foundries adopt RF SOI, increase of ICs area

1992 — 2003 — 2005 — 2011 — 2012 — 2014 — 2020

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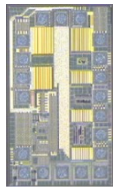
- **UCL R&D work on HR-SOI**



RF switch demo on **HR-SOI**

Trap Rich SOI by UCL and Soitec

HR-SOI High Volume Manufacturing

eSI™ ramp

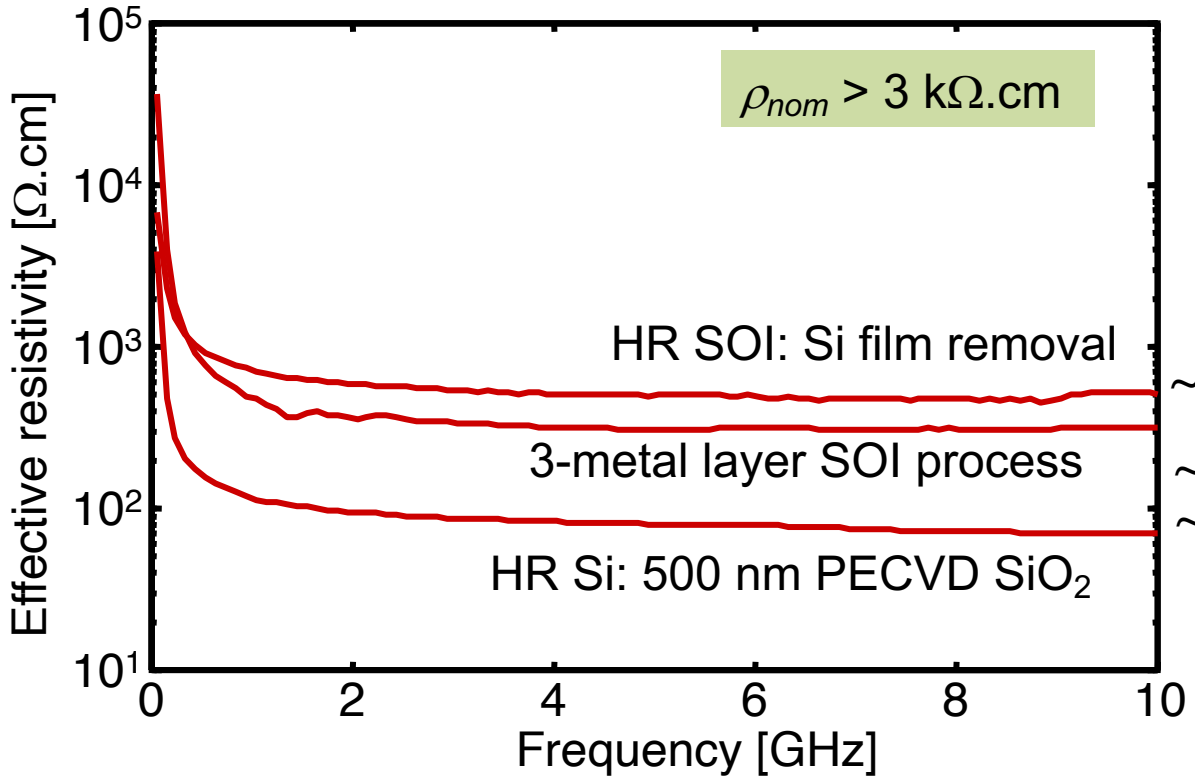
RF switch on **SOI** becomes industry **mainstream**

1st Power Amplifier on RF-SOI

> 40 mm² of **RF SOI** chips in smartphone

2004: Question from SOITEC to UCLouvain

soitec



Typical ρ_{eff} values

~ 500 Ω.cm

~ 250 Ω.cm

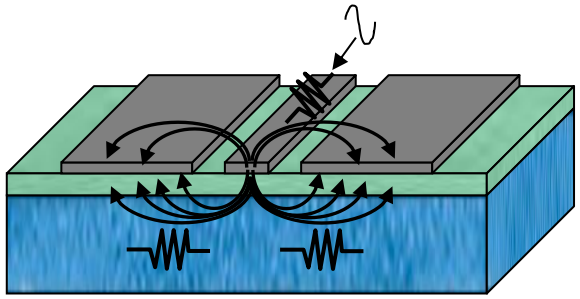
~ 80 Ω.cm

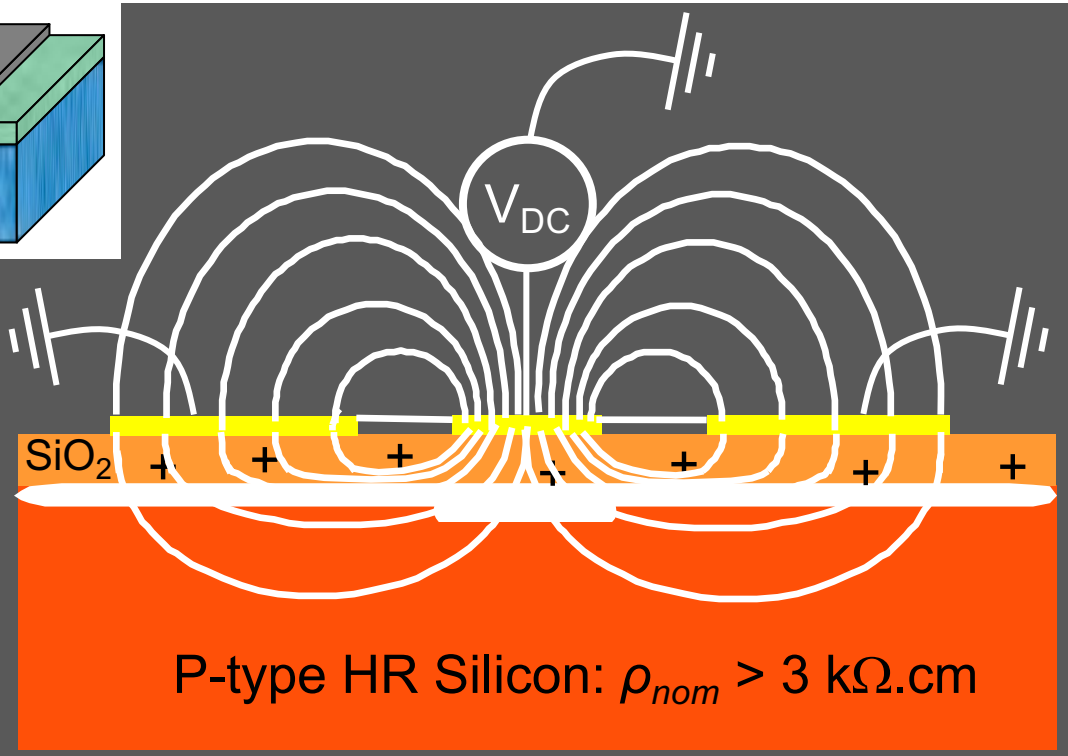
- Effective resistivity **depends on process**
- Effective resistivity is **lower than 3 kΩ.cm**

WHY?

[D. Lederer, J.-P. Raskin, *IEEE EDL'05*]

Parasitic Surface Conduction (PSC)





PSC caused by:

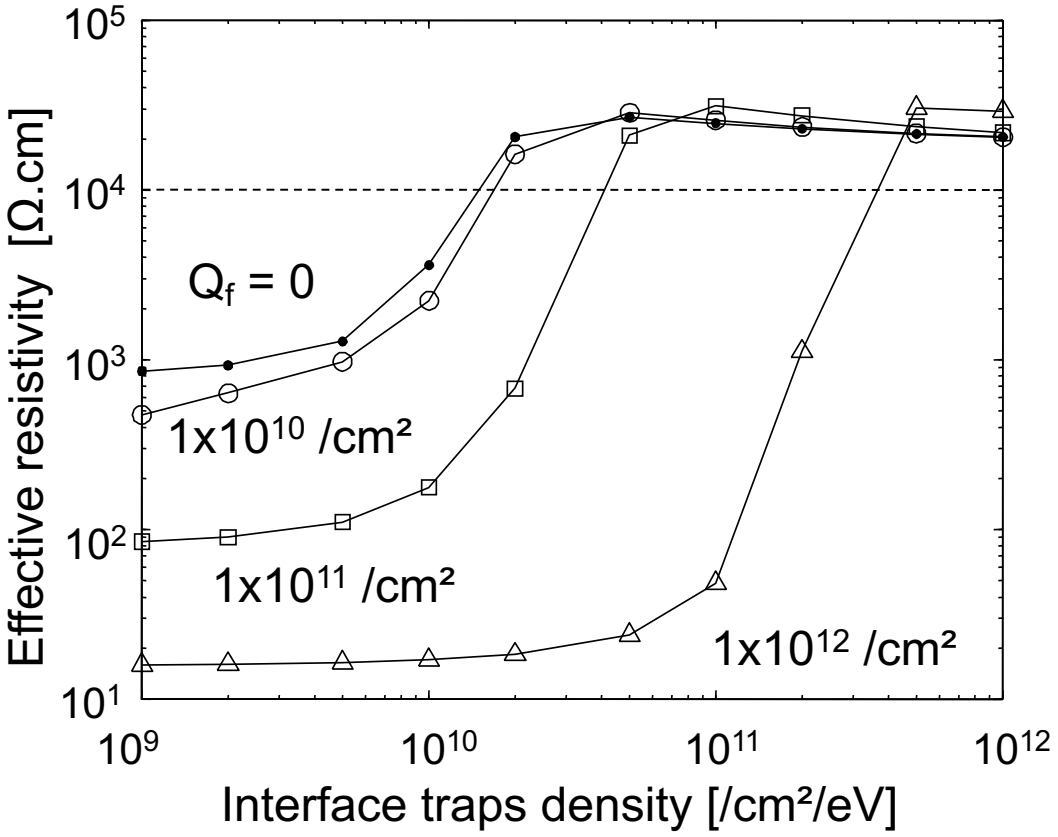
- fixed charges (Q_f) in the oxide (BOX of SOI, IMD layers)
- Bias applied on the metallic conductors

For oxidized HR Si:

- *Effective* resistivity lower than *nominal* resistivity
- Substrate losses higher than expected (coplanar devices)

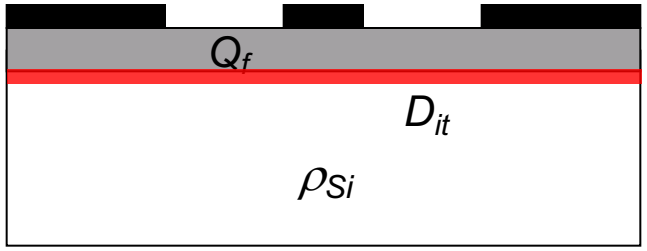
Dependence of the effective resistivity

$$\rho_{eff} = f\,(\,\rho_{Si}\,,\; Q_f\,,\; t_{ox}\,,\; V_a\,,\; D_{it}\,)$$



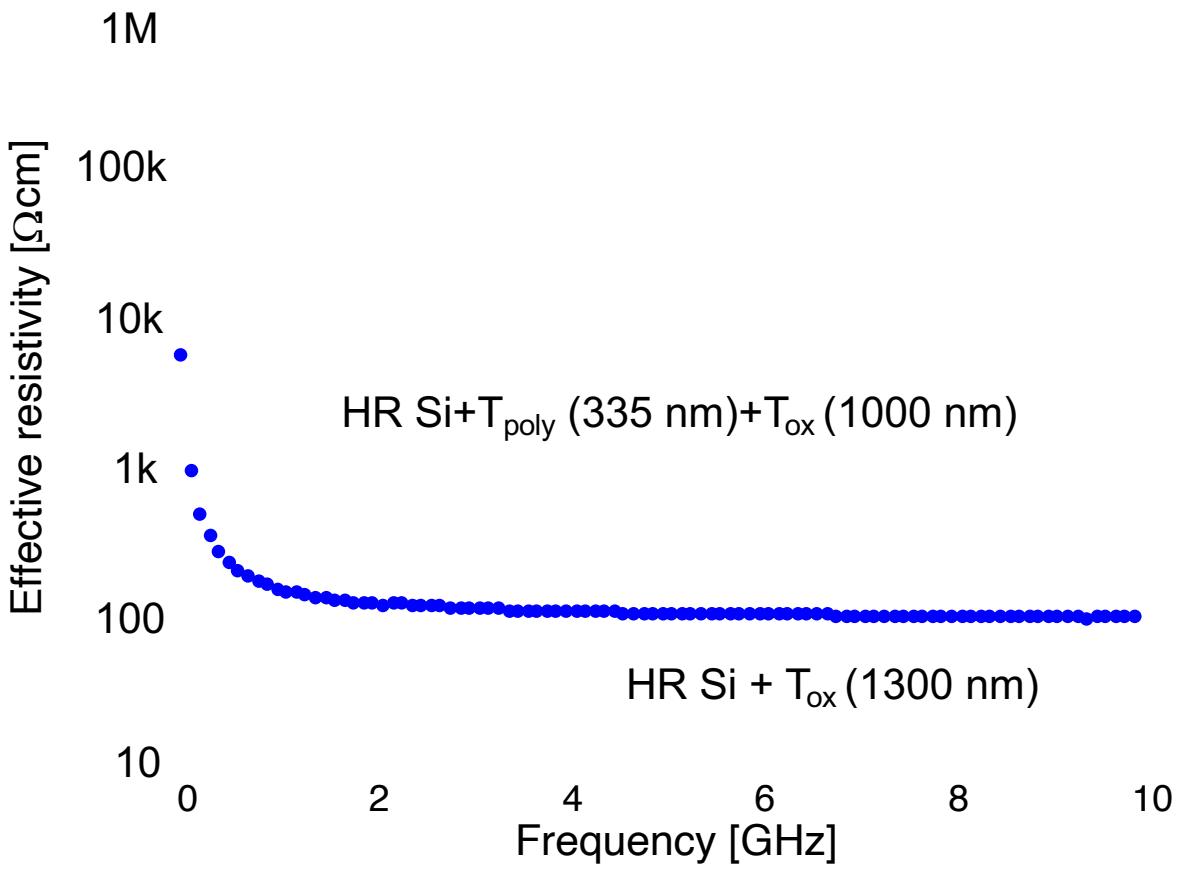
$D_{it} \sim 10^{12}$ /cm²/eV

for being independent of Q_f,
and then reach the
high resistivity behavior



Experiments in our academic clean room facilities – it works!

Effective resistivity of CPW: ~10 kΩ.cm



[D. Lederer, J.-P. Raskin, *IEEE EDL'05*]

2005: fundamental academic breakthrough

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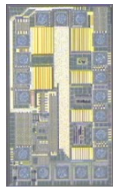

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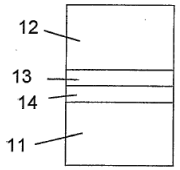

Trap Rich SOI by UCL and Soitec

Patent

Dr. Dimitri Lederer

HR-SOI High Volume Manufacturing

eSI™ ramp

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2008: call from Qorvo – substrate linearity

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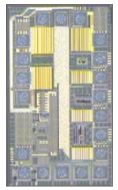

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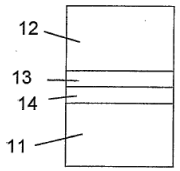

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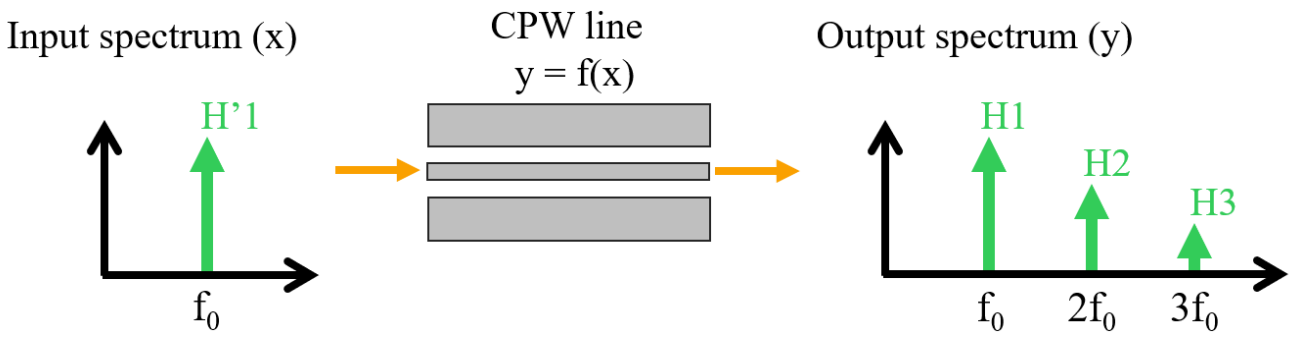
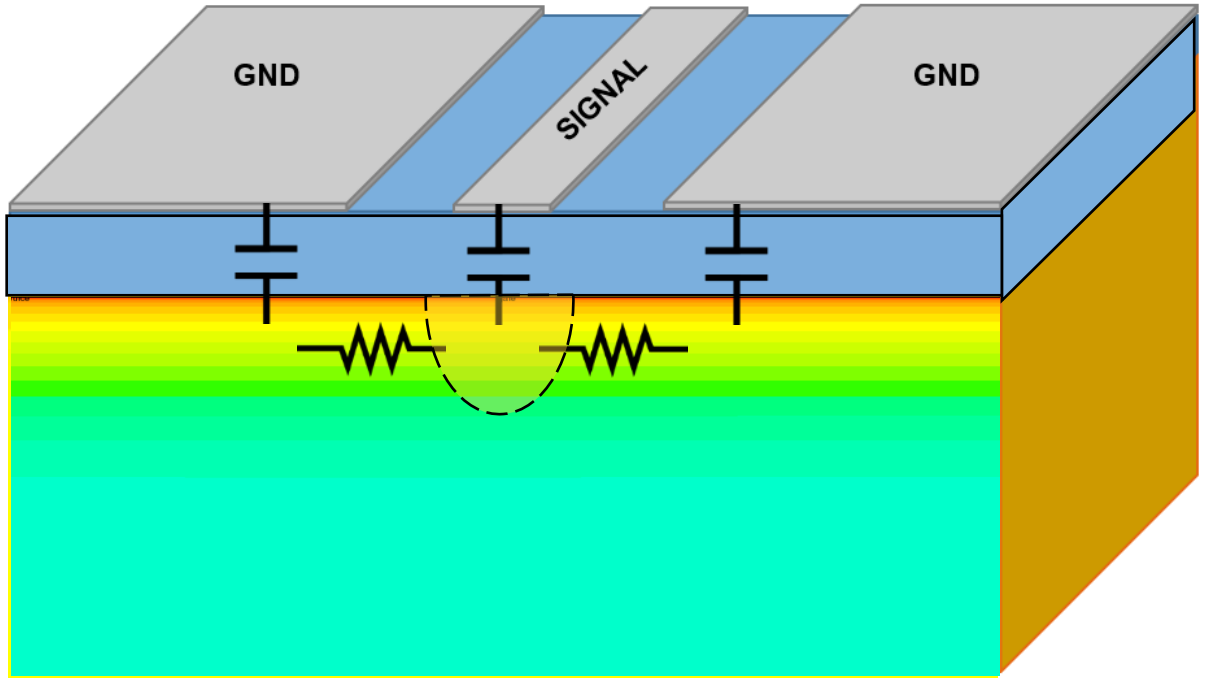
Si Substrate – Source of non-linearity



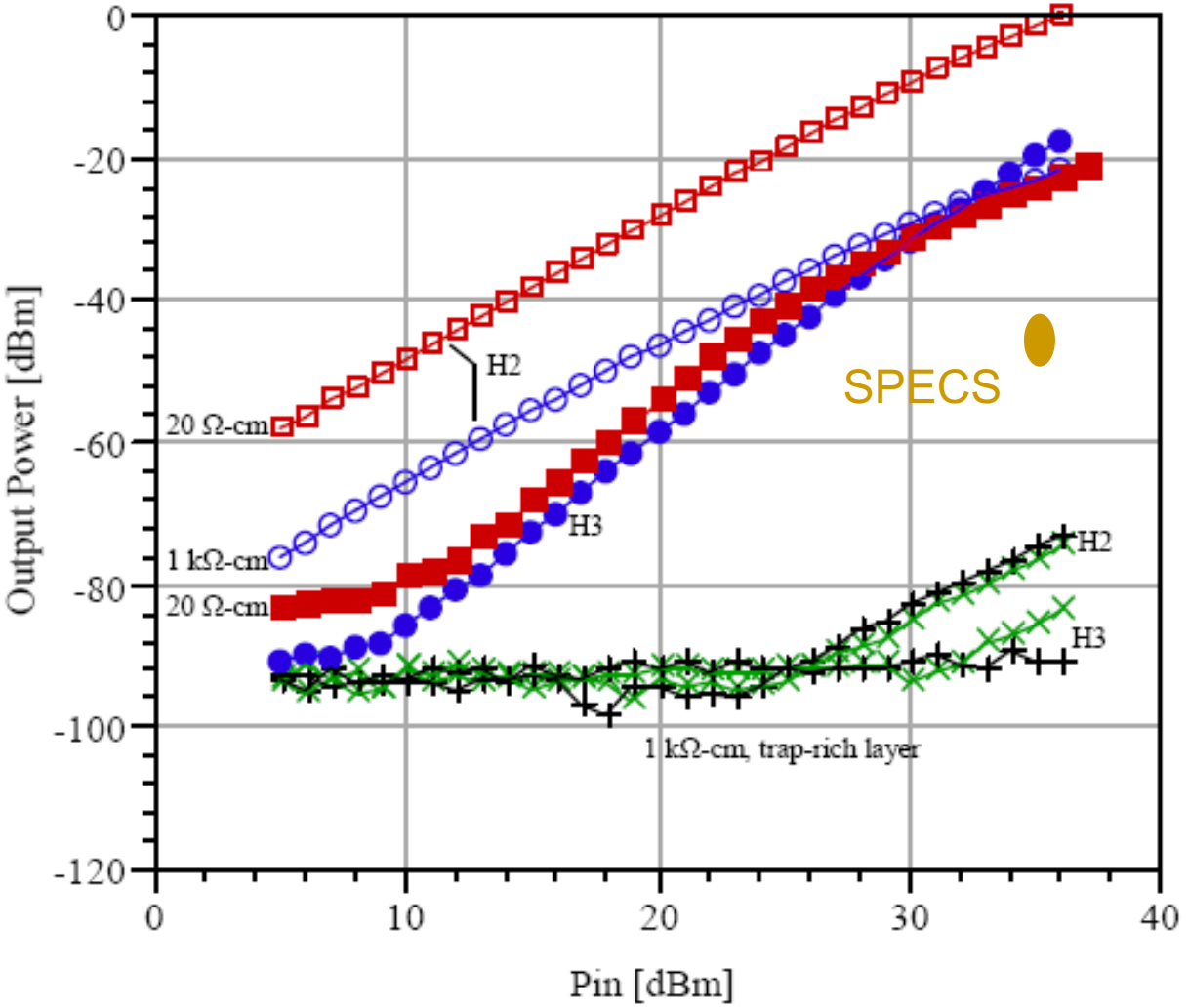
Ideal linear transfer function: $y = f(x) = a \cdot x$

Real non-linear transfer function: $y = f(x) = a \cdot x + b \cdot x^2 + c \cdot x^3 + \ldots$

Semiconductors are non-linear by nature (field-effect)



2008: drastic reduction of the substrate non-linearties



-60 dB

[D. Kerr, C. Roda Neve, J.-P. Raskin, *SiRF'08*]

[C. Roda Neve, J.-P. Raskin, *IEEE TED'13*]

2008: a long journey to industrialization

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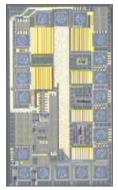

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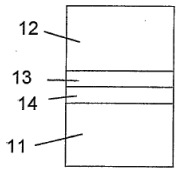

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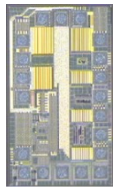

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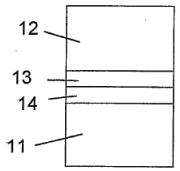

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Dr. Mostafa Emam

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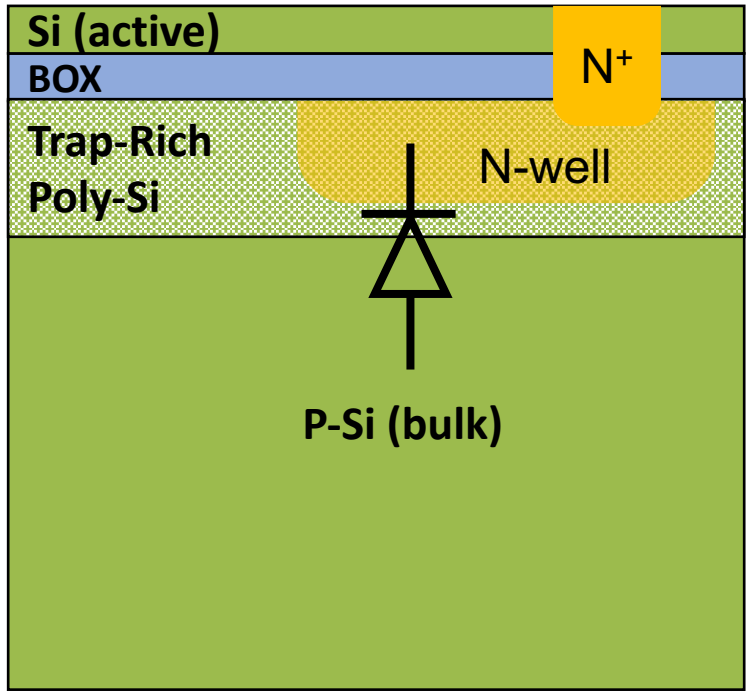
incize

15-20 years from discovery to products innovation

Move to 5G, 6G, …

- Move to **low power mmW frequencies**: need for shorter nodes
- Move from **PD SOI to FD SOI**
- What about the **compatibility of trap-rich** RF-SOI substrate **with FD SOI?**

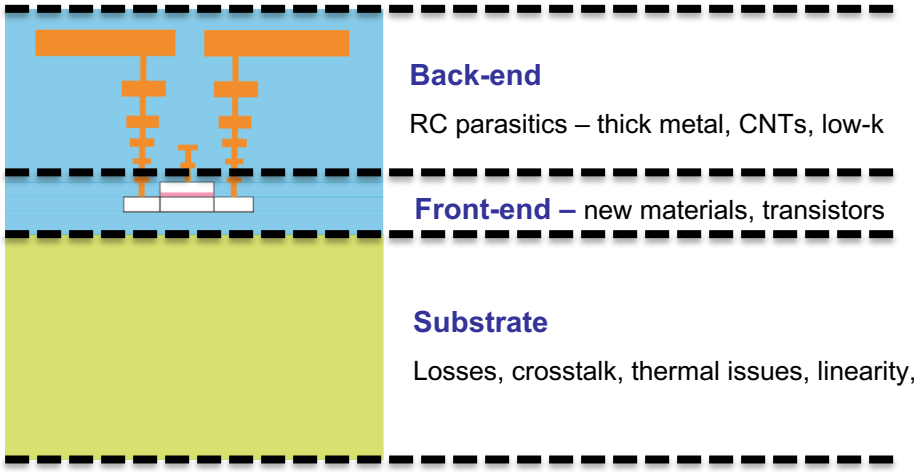
Compatibility of trap-rich concept with FD SOI technology?



FD-SOI offers **functionalities below the BOX**.

Back-gates and isolation diodes will then be defined **in the trap-rich** polysilicon.

Much larger reverse leakage current of PN junction in polysilicon layer.



Back-end

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Front-end – new materials, transistors

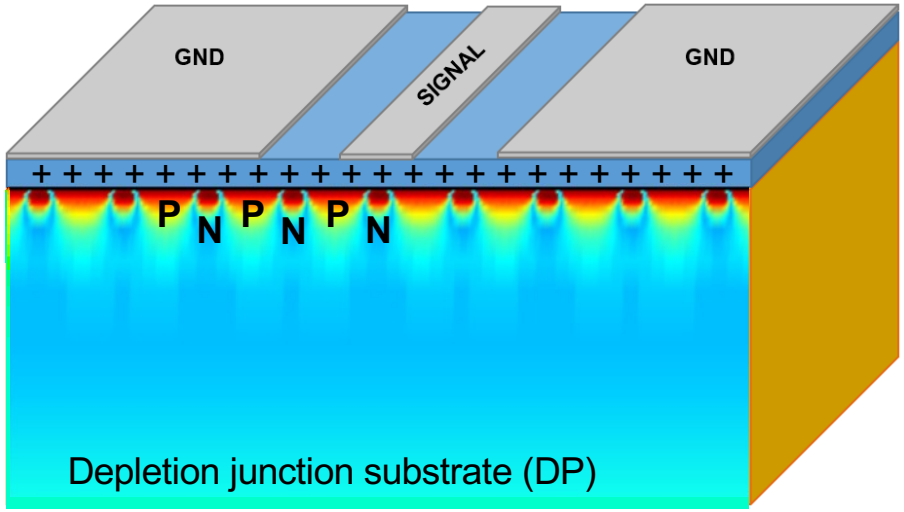
Substrate

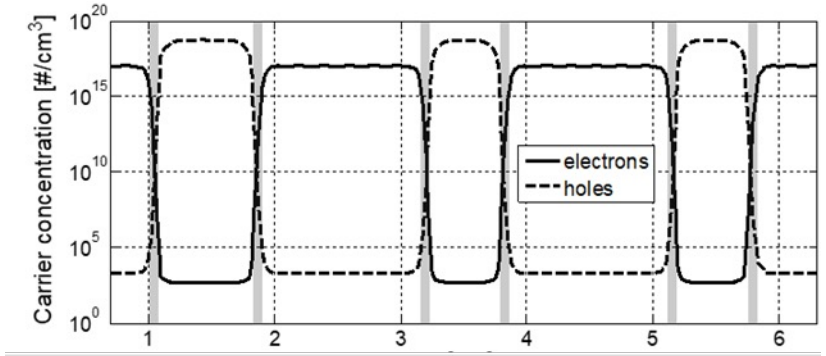
Losses, crosstalk, thermal issues, linearity, …

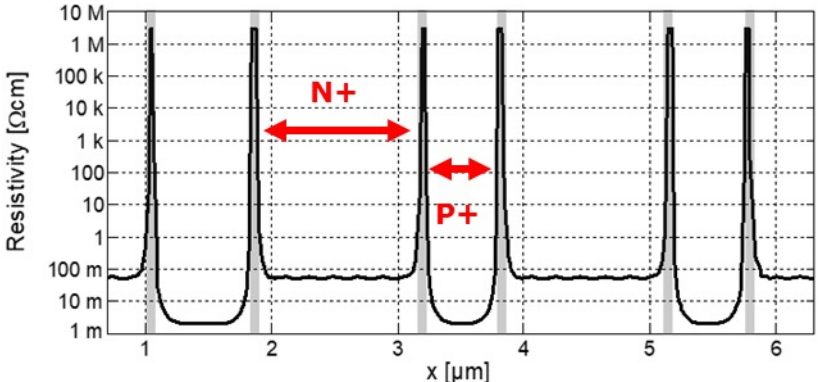
New generations of innovative SOI substrates for RF and mm-waves applications

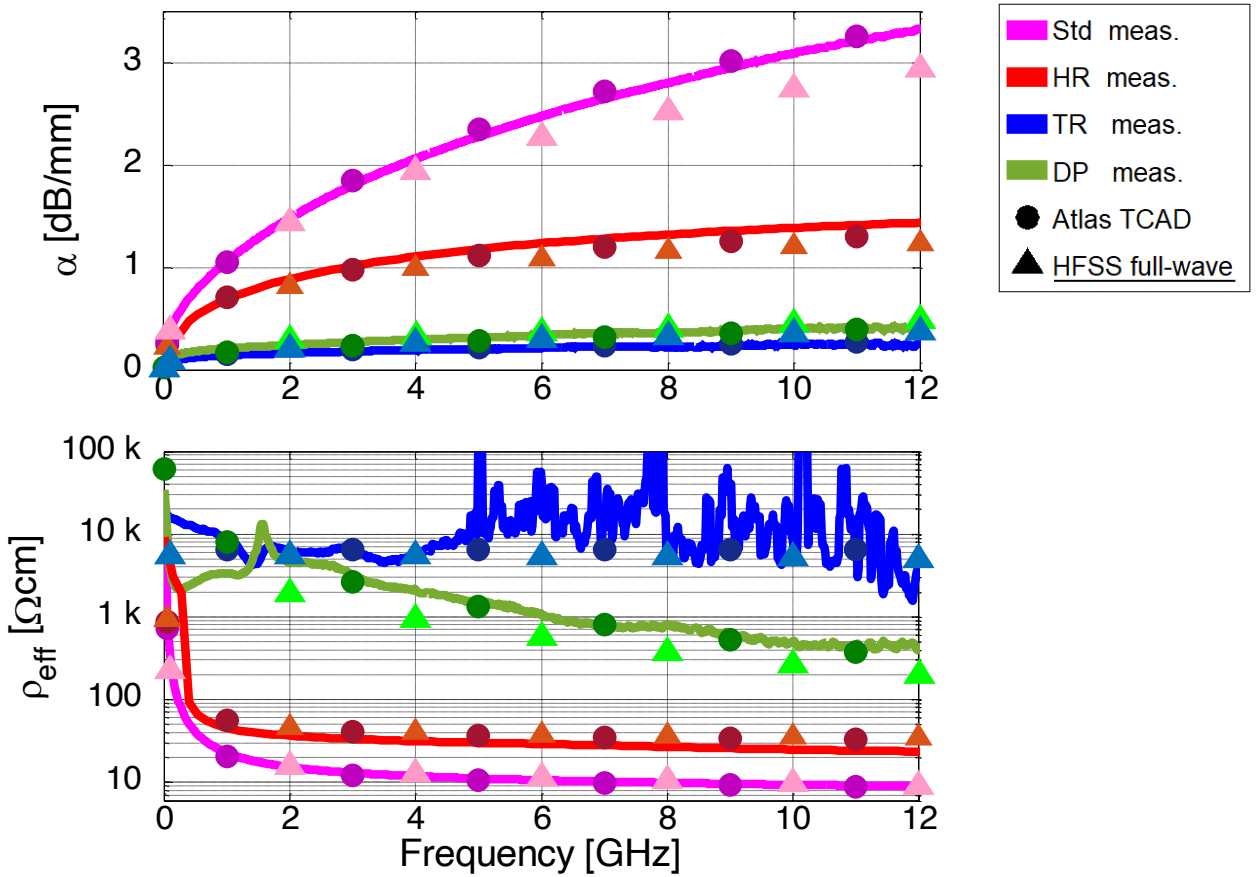
Smart PN junctions implanted below the BOX

Deep depletion – Smart PN implants



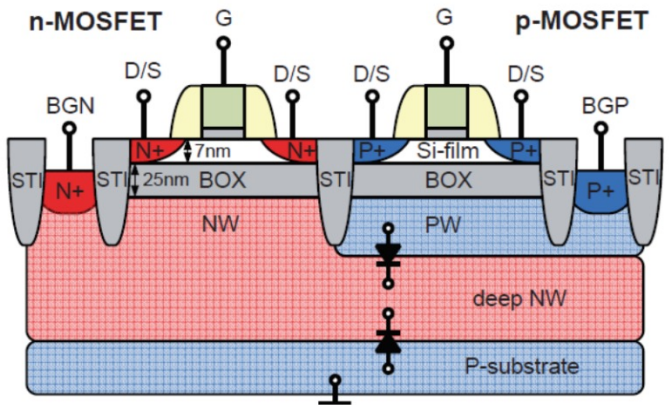






[M. Rack *et al.*, *IEEE Electron Device Letters*, May 2019]

Smart PN implants – compatible with FD SOI

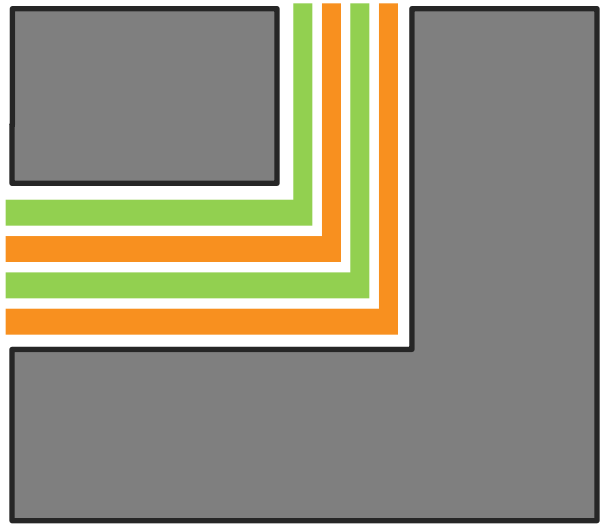


GLOBAL FOUNDRIES

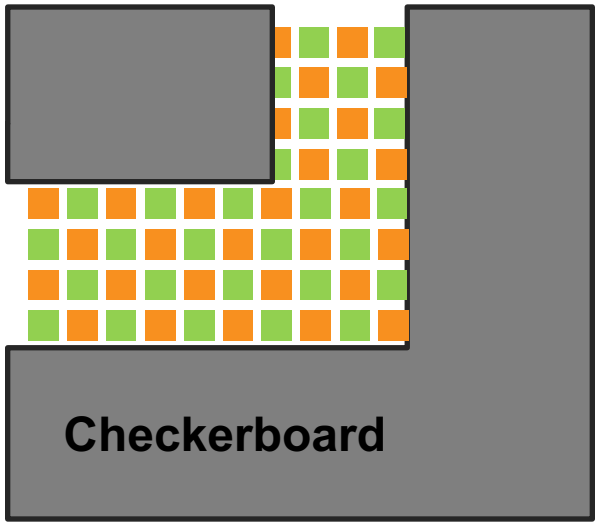
life.augmented

Techno layer
P implant
N implant

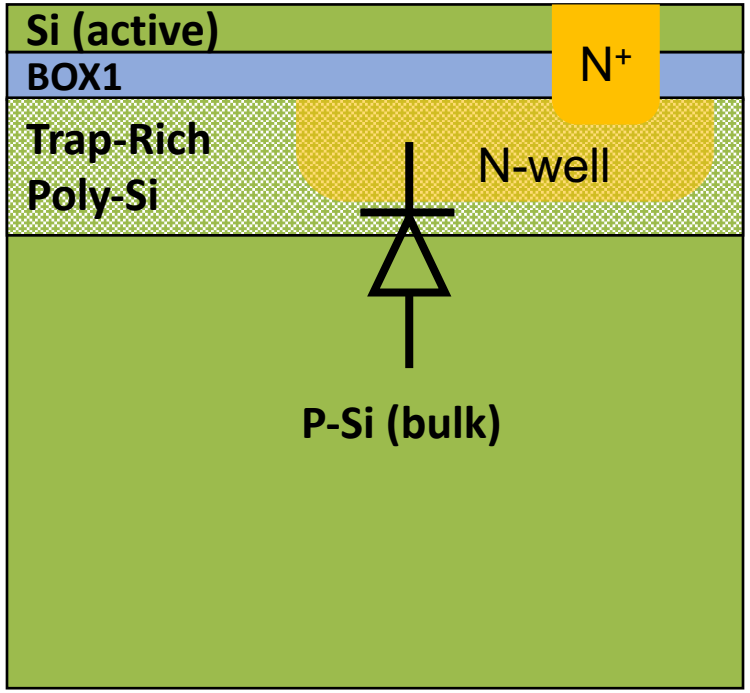
Co-design between circuit layers and substrate layers



Independency between circuit layers and substrate layers



Double BOX SOI substrate for enhanced digital and RF functionalities



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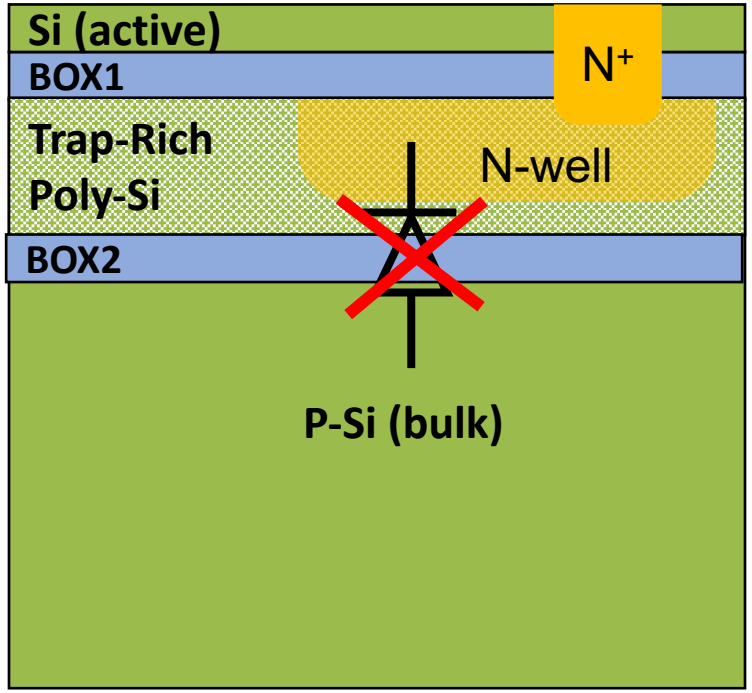
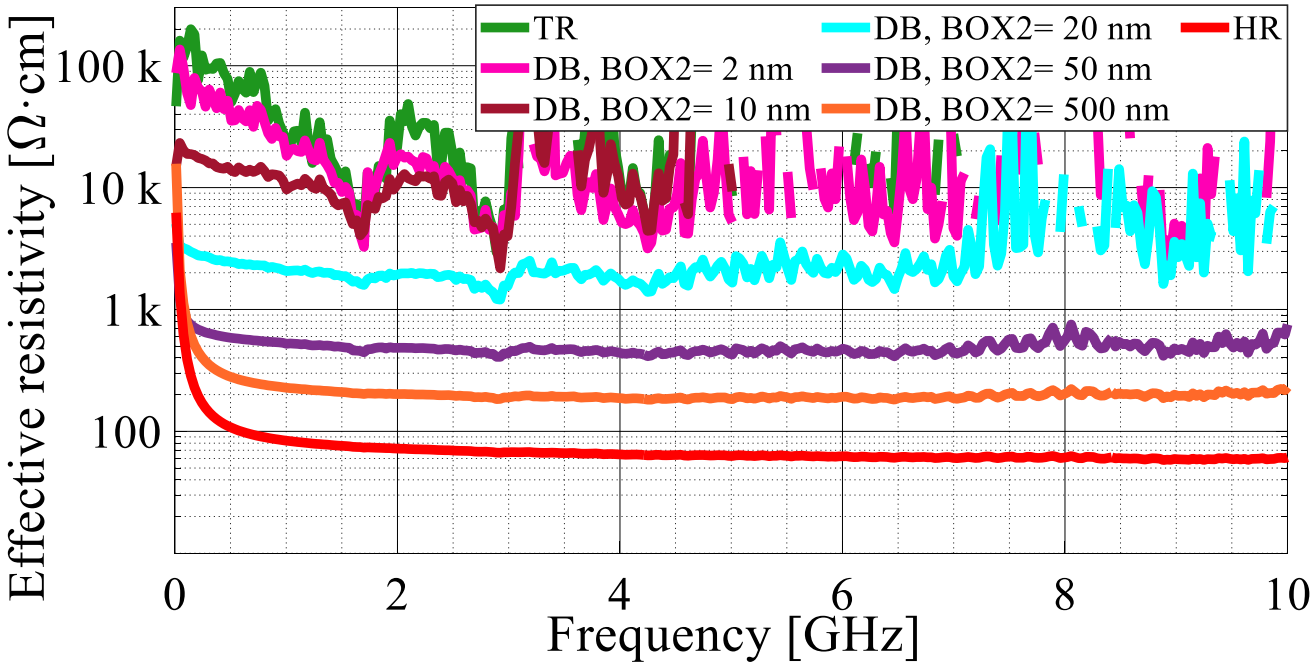


Effective Resistivity



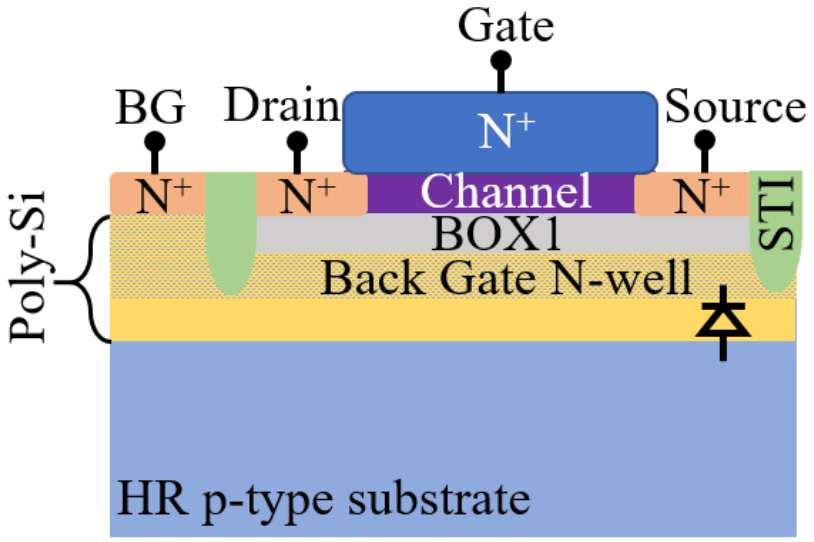
Measured effective resistivity as a function of the frequency for the TR, HR and DB substrates with different BOX2 thicknesses.

With the **increase in BOX2 thickness**, the trap-rich polysilicon layer becomes further away from the BOX2-bulk interface, and the **passivation is less effective**.

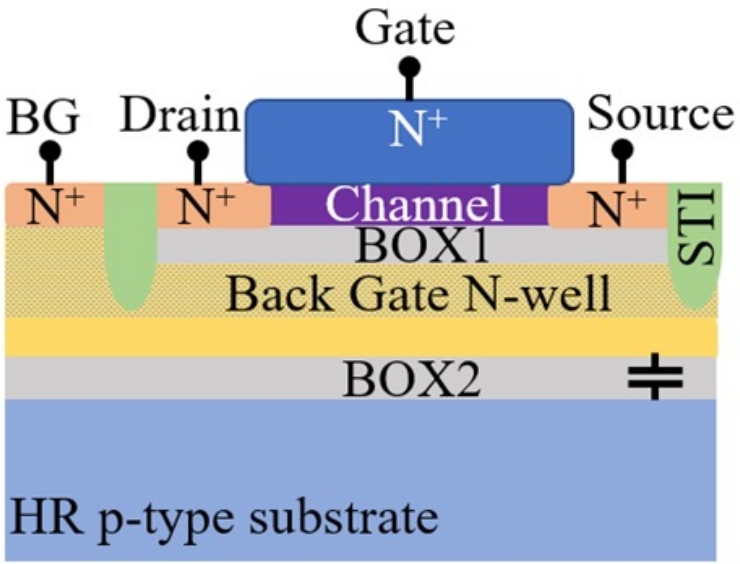
If the BOX2 thickness is **thinner than 10 nm**, the **effective resistivity** of the substrate is at least equal to **10 kΩ·cm**.

Therefore, it demonstrates that DB wafer can be **as efficient as TR wafer** if BOX2 is thinner than 10 nm.

Digital and RF enhanced features



(a)



(b)

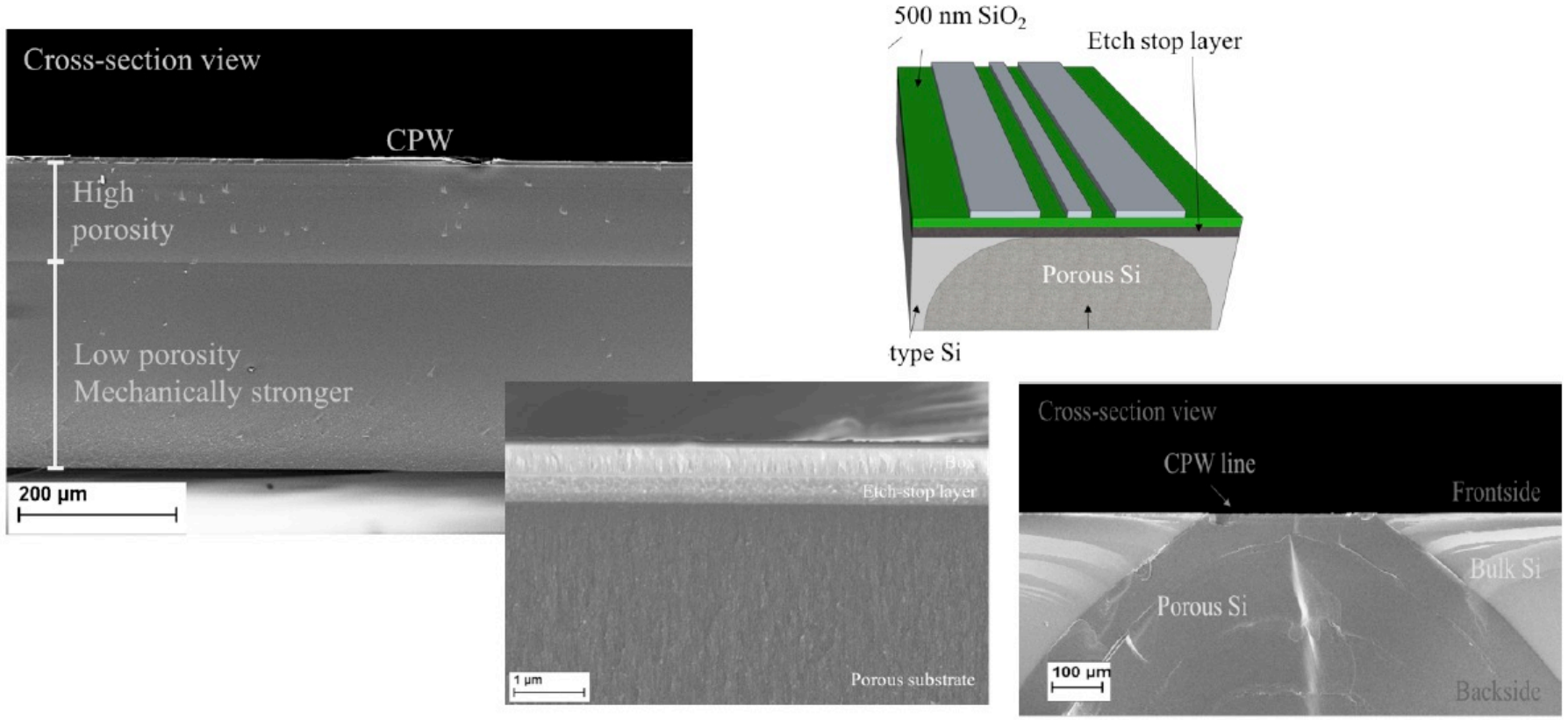
- **DB SOI** substrate combined with high-resistivity handle Si wafer exhibits **RF performance similar to the best TR SOI** if **BOX2 is thinner than 10 nm**.

- Thanks to **BOX2 layer**, **TR** can be implemented beneath BOX1 **without degrading the isolation** of the back gate with the handle Si substrate.

- DB SOI substrate offers much **larger back gate voltage tuning range** thanks to the presence of BOX2 layer underneath the back gate contact. This feature is quite **interesting for digital circuits**.

Backside porosification of SOI substrate

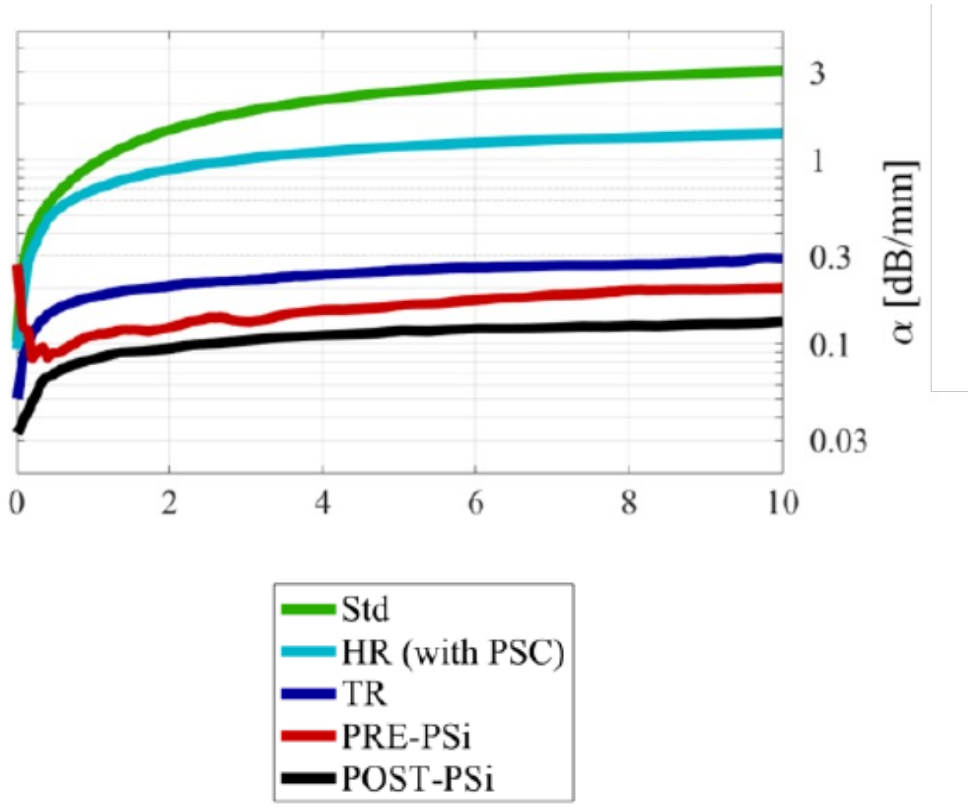
Porous Silicon in post-CMOS

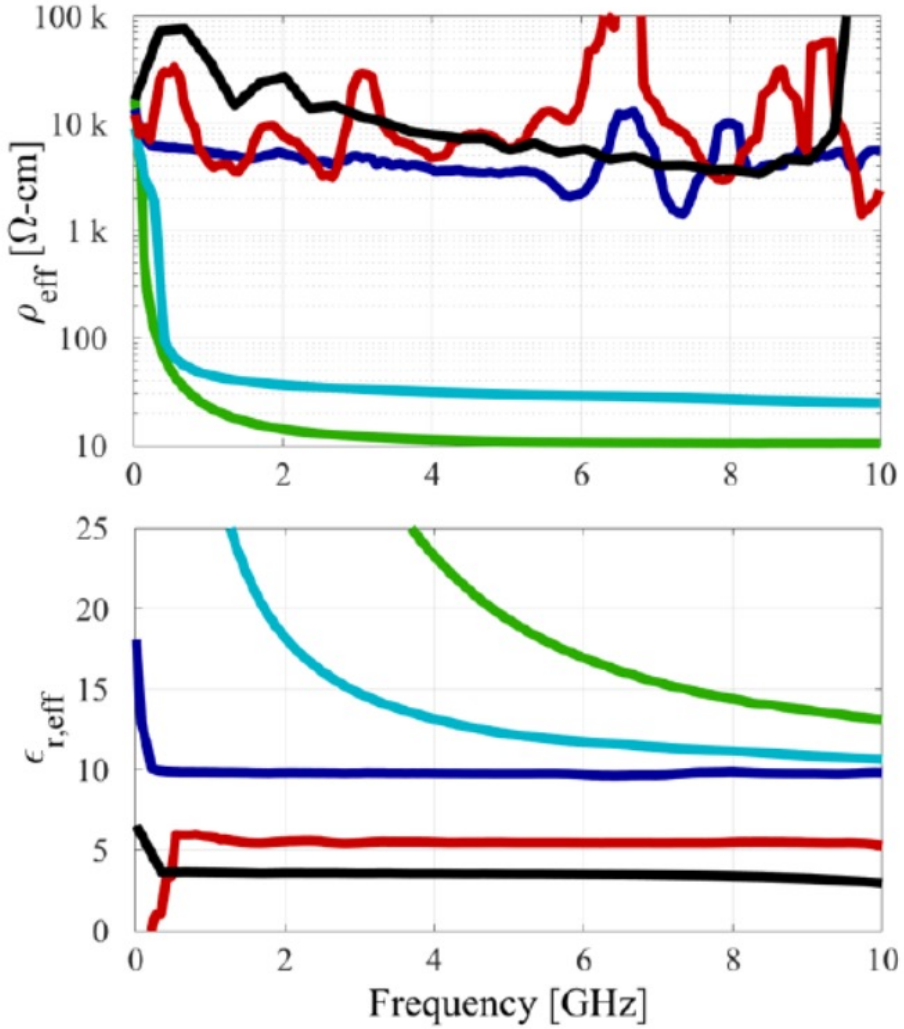


[G. Scheen *et al.*, *IEEE International Microwave Symposium 2019*]

[M. Rack *et al.*, *IEEE Transactions on Electron Devices*, May 2018]

Porous Silicon – RF performances

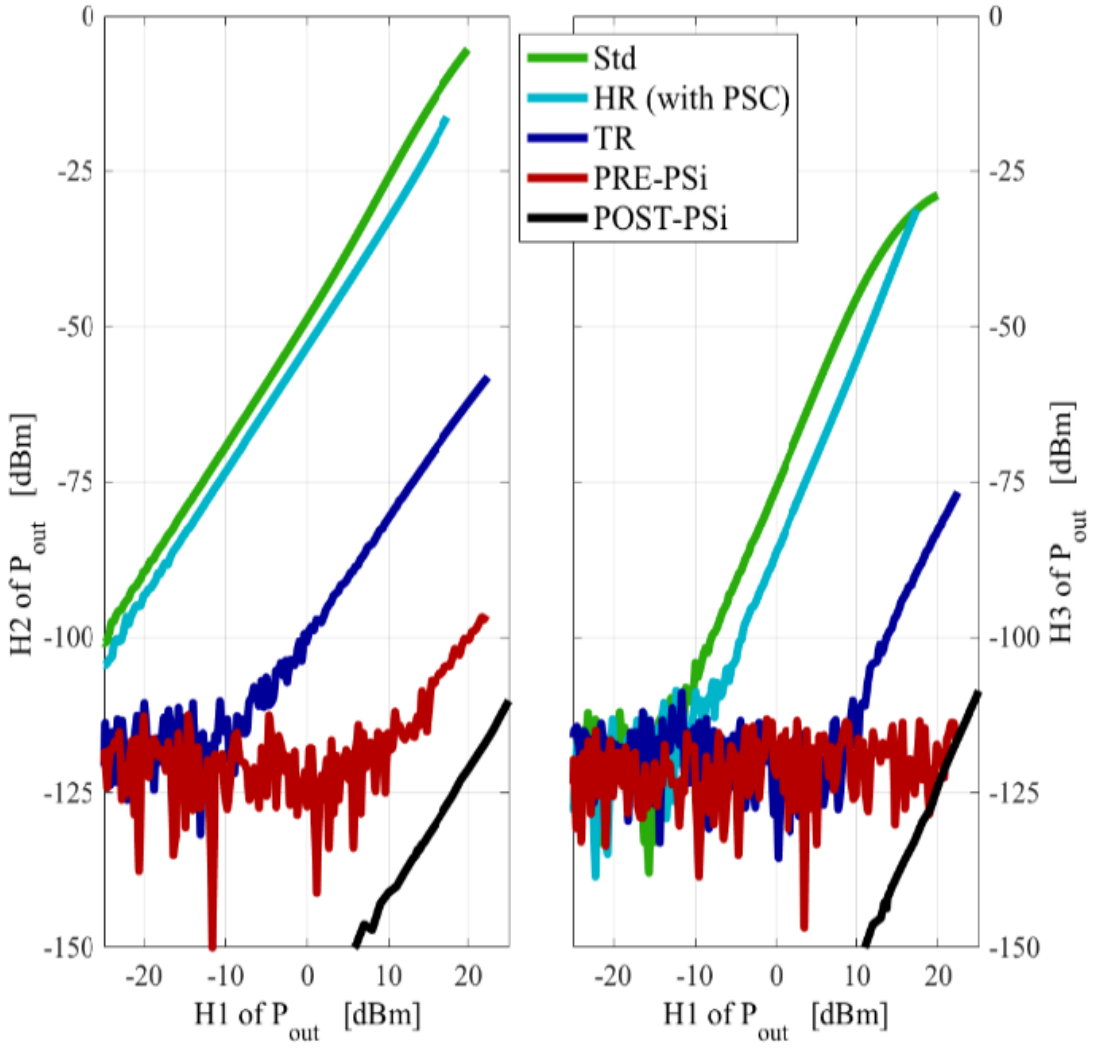




[G. Scheen *et al.*, *IEEE International Microwave Symposium 2019*]

[M. Rack *et al.*, *IEEE Transactions on Electron Devices*, May 2018]

Porous Silicon – RF performances



Linearity

TR-SOI

-75 dBm

POST Porous Si

-130 dBm

[G. Scheen *et al.*, *IEEE International Microwave Symposium 2019*]

[M. Rack *et al.*, *IEEE Transactions on Electron Devices*, May 2018]

Conclusions

- **Trap-rich HR SOI (eSI)** presents outstanding RF performance. There is still room for improvement and innovation;
- **The benefits of HR Si substrate for FD SOI have been demonstrated.** In that case, smart PN implants underneath the thin BOX are used to get rid of the parasitic surface conduction and thus conserve the HR properties of the substrate;
- **Double BOX SOI** substrate demonstrated enhanced digital and RF functionalities;
- **Porous Si** in post-CMOS leads to substrates characterized by a very **high effective resisitivity** and **low permittivity**;
- Today, smart-cut is used to transfer **GaN** or **InP** on top of **HR Si substrate** for serving the **high power and high frequency** ICs at RF and mmW.

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