



RFSOI : How did we get here and where are we headed?

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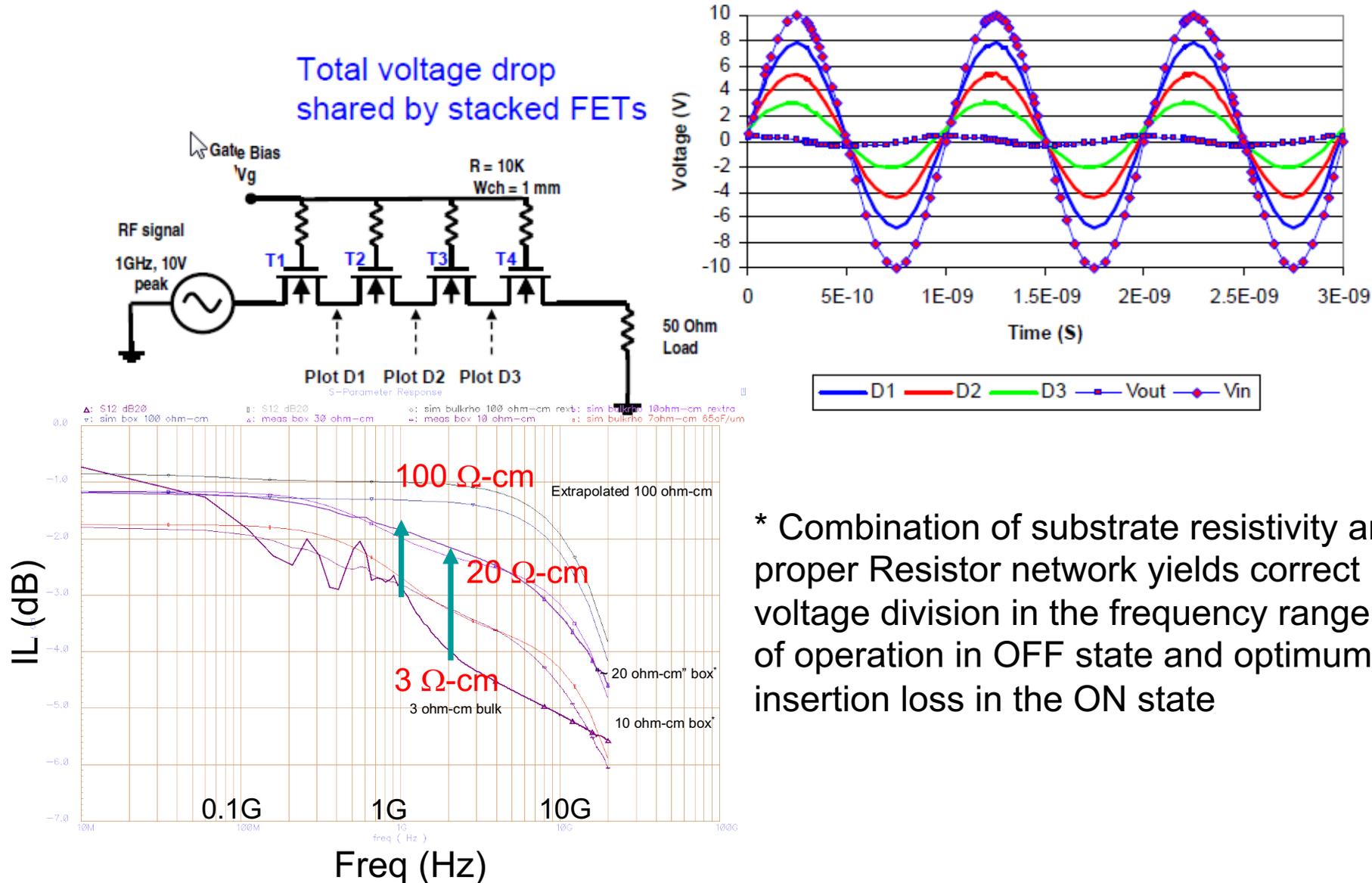
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RFSOI Transistor Stacking Concept

- The need for high resistivity silicon substrates was realized very early. Without HiRES silicon substrates at low cost, RFSOI would never have succeeded!

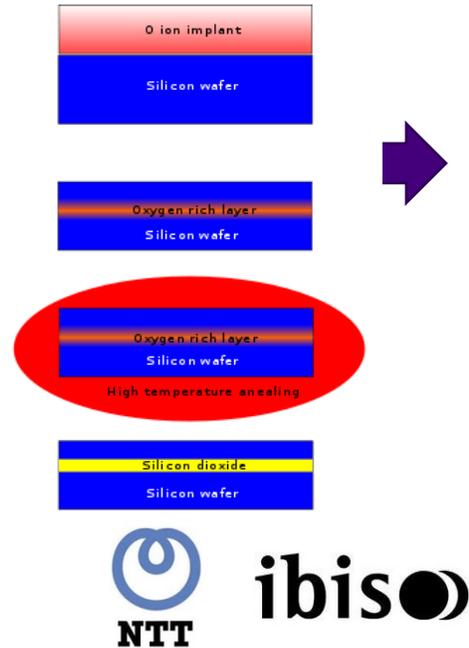


* Combination of substrate resistivity and proper Resistor network yields correct voltage division in the frequency range of operation in OFF state and optimum insertion loss in the ON state

Chronology of RFSOI Technology Development

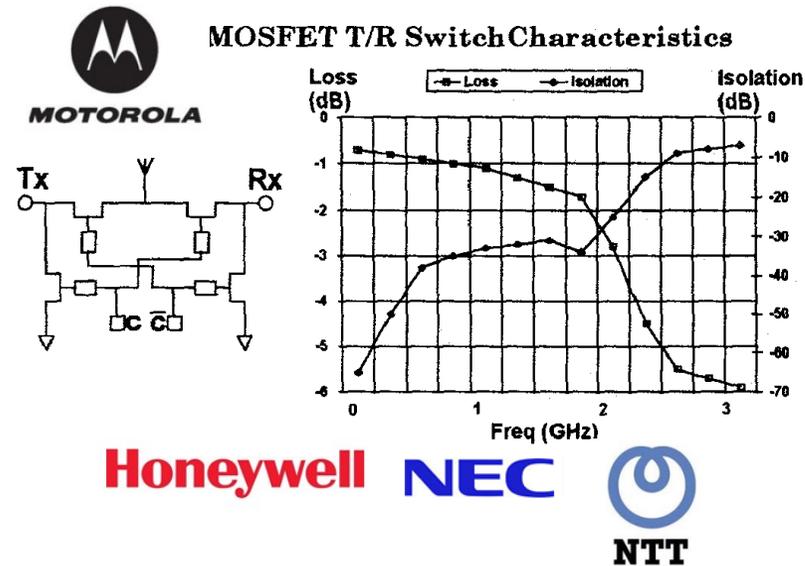
- Critical technology breakthroughs allowed RFSOI to be omnipresent in today's handsets

1990



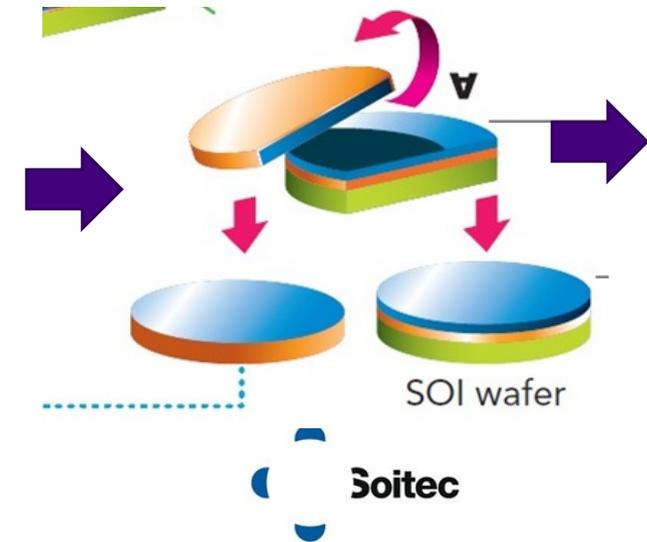
- SIMOX substrates introduced
- 50% speed/power improvement over bulk
- RD -> production

1995



- Demonstration of fully integrated switches / RFIC / controllers
- Performance limited by lack of low-cost High Res silicon substrate
- SIMOX yields problematic for large volume product

Early 2000's

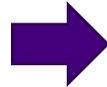


- SmartCut process dramatically improves yield and drives digital volume
- Low Cost 1000 Ohm-cm silicon substrates introduced
- RFSOI foundry development starts

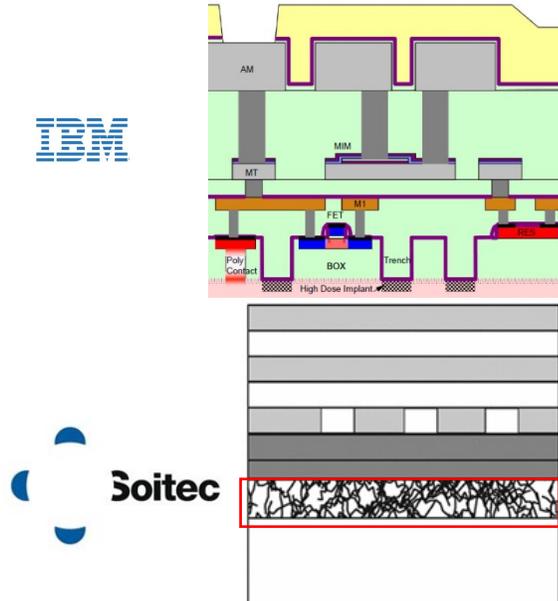
Chronology of RFSOI Technology Development

- Critical technology breakthroughs allowed RFSOI to be omnipresent in today's handsets

Mid 2000's



Late 2000's



>2024



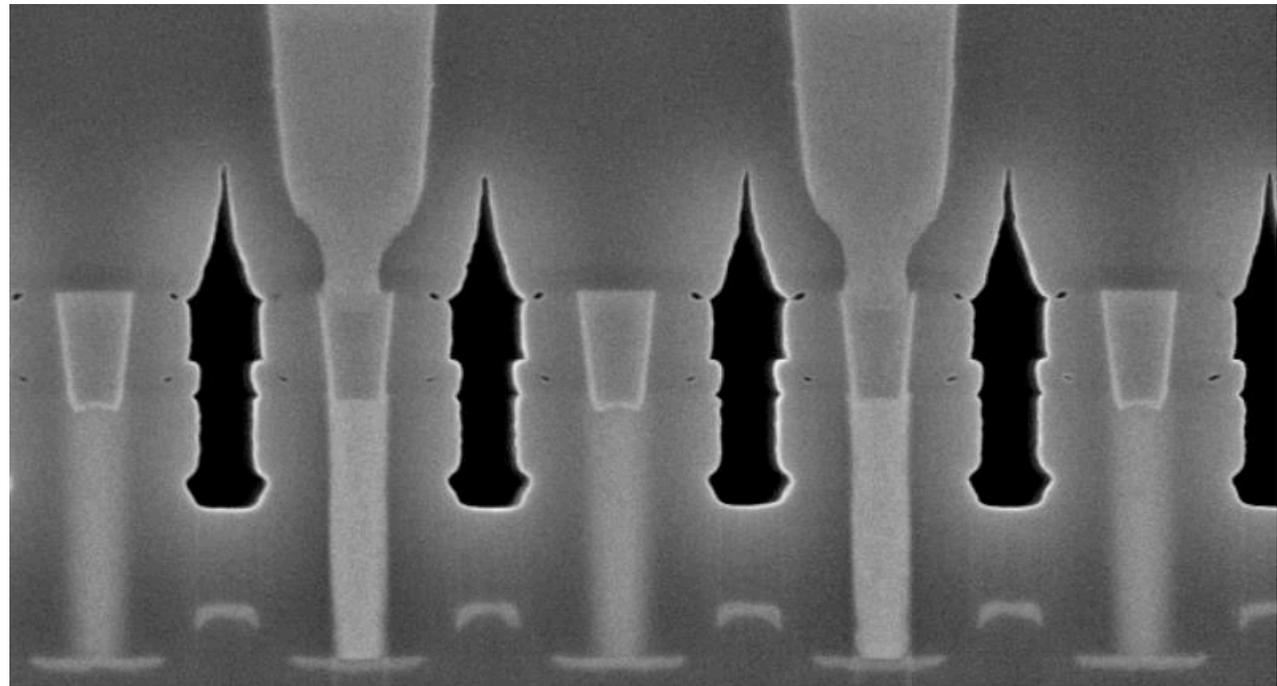
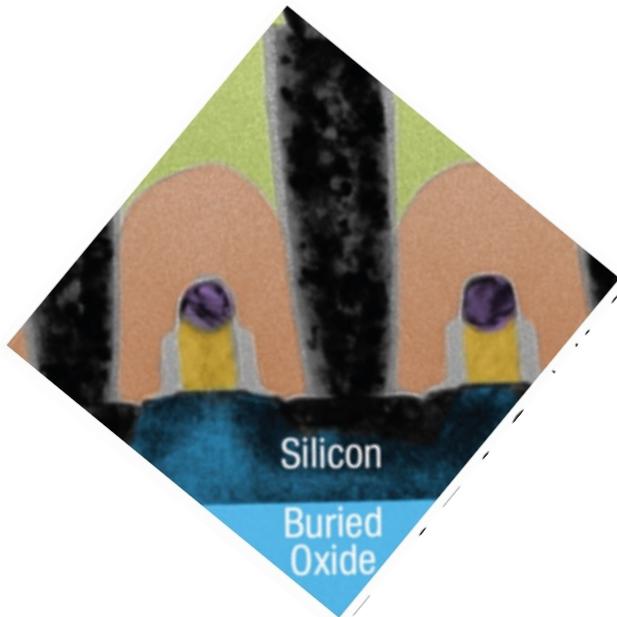
- Silicon foundries offer RFSOI technologies
- Rapid proliferation of design groups worldwide
- Linearity still limited by silicon substrate surface interface effects

- Two distinct surface treatment approaches nearly eliminate substrate surface effects:
 - Handle Wafer Treatments
 - Trap Rich Interface Layer

- >2B US\$ RFSOI market
- Wafer Capacity > 1Million WPY
- High performance switches and Tuners
- Participation in 100% of 4G /5G handsets and devices

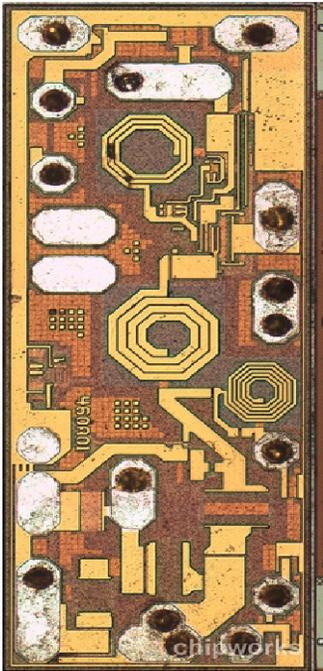
The modern RFSOI Switch Transistor

- PDSOI (Partially Depleted SOI) channels for optimal body control at high VRMS voltages
- Gate lengths $L_g < 120\text{nm}$
- Epi thickness $< 1000\text{\AA}$
- Air Gap technology to reduce COFF
- Combination of lithography layers to optimize performance and cost.

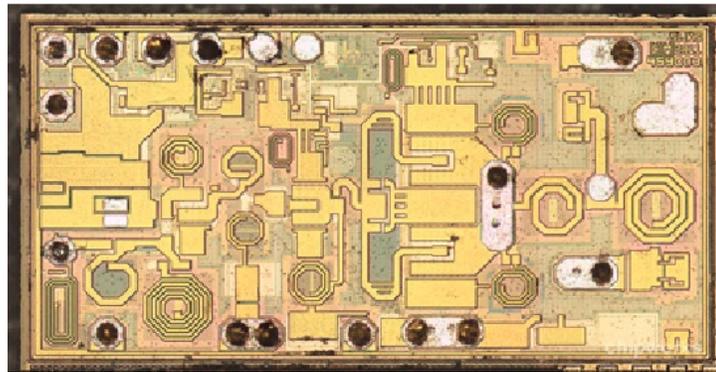


Integration of Passive Devices

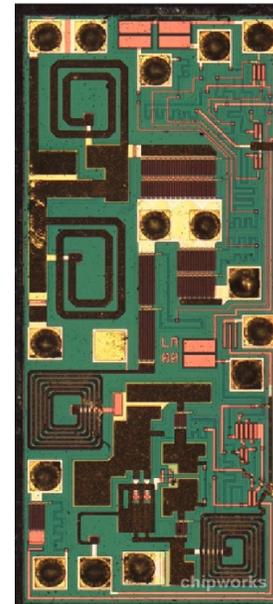
- RF integration of passives is essential for reduced overall system cost
- Precision Passive devices account for more than 60% area and cost
- Inductors/transformer metrics are critical → Limit the overall circuit performance



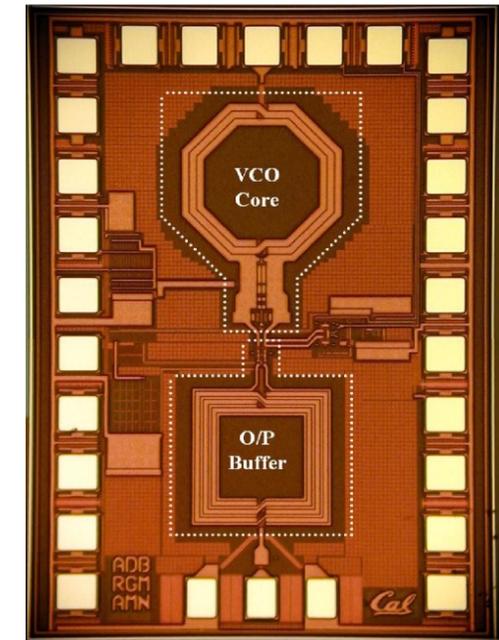
5 GHz LNA¹



5 GHz PA¹



2.4 GHz BPF¹



1.8 GHz VCO²

1- <http://www.chipworks.com/about-chipworks/overview/blog/apple-iphone-5-the-rf/>

2 - https://buffy.eecs.berkeley.edu/PHP/resabs/resabs.php?f_year=2004&f_submit=one&f_absid=100326

9SW Technology: GF RFSOI Evolution

- Over 1 million RFSOI wafers shipped

Continuous enhancements in performance, integration, area and cost.



7RF SOI
12 μm Cu BEOL

7RF SOI
5 V CMOS
DGnFET LNA
50 V Vncap

7RF SOI
“LowD” Low-IMD switch
NoBTQ

7SW SOI
✓ 30% improvement in Ron-Coff*
✓ Up to 30% smaller die*
✓ Trap Rich SOI Substrates

8SW SOI
✓ 300mm technology
✓ Airgap to lower Coff
✓ Ron-Coff* < 100fs
✓ 130nm CMOS
✓ State-of-the-art LNA

9SW SOI
✓ 300mm technology
✓ Ron-Coff* < 80fs
✓ Improved 90nm digital density/performance
✓ Dual Airgap module



2008

2011

2012

2013

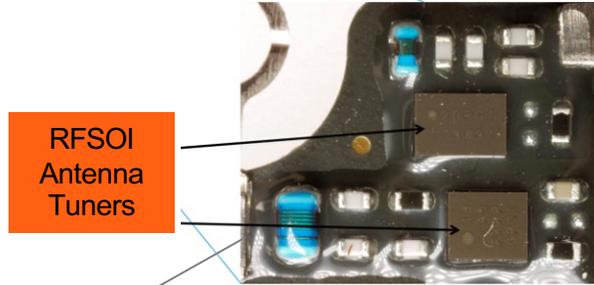
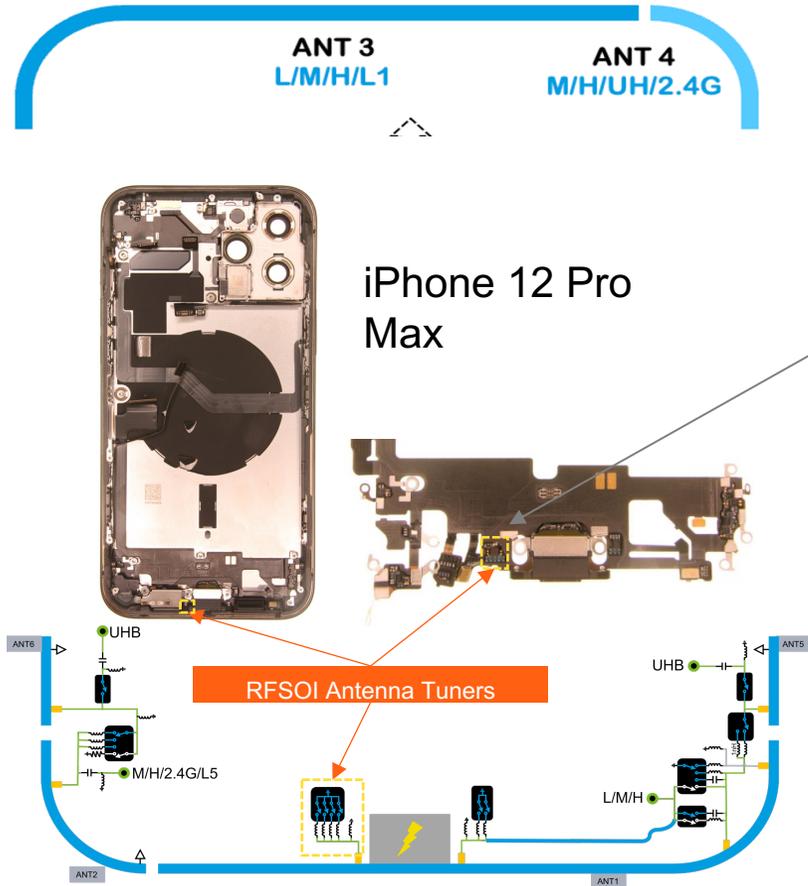
2014

2018

2023

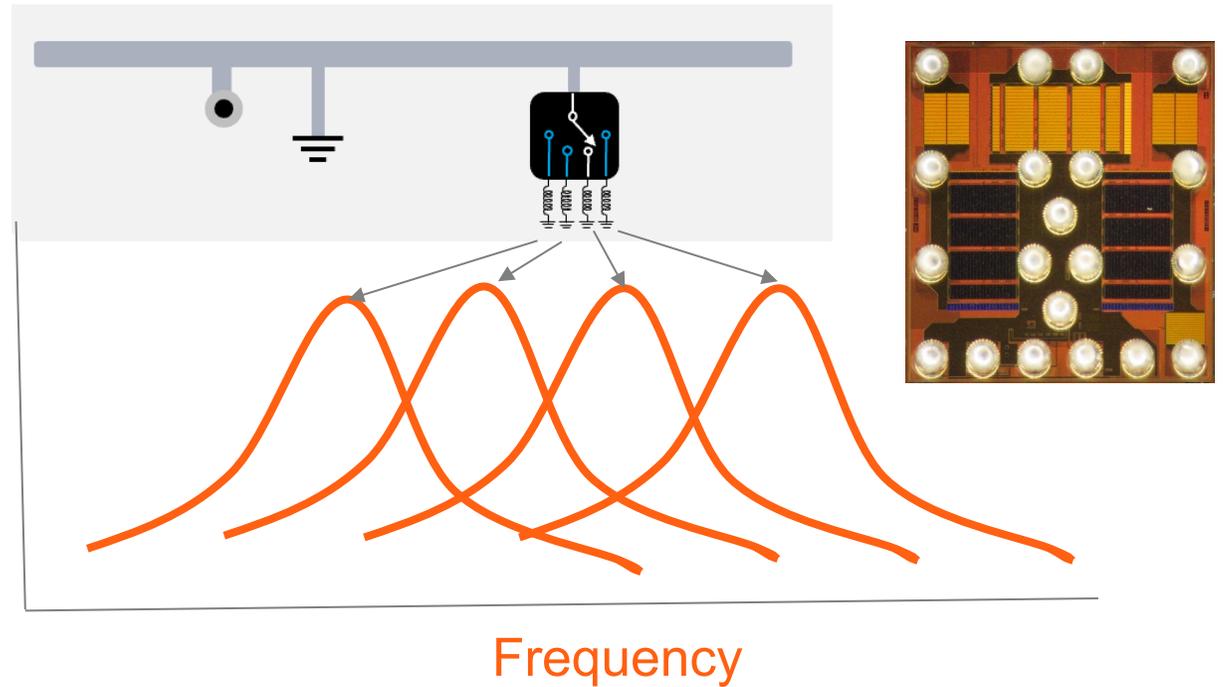
RFSOI Antenna Tuners

- Improve Antenna Efficiency for the plethora of bands in mobile handset = battery usage efficiency!



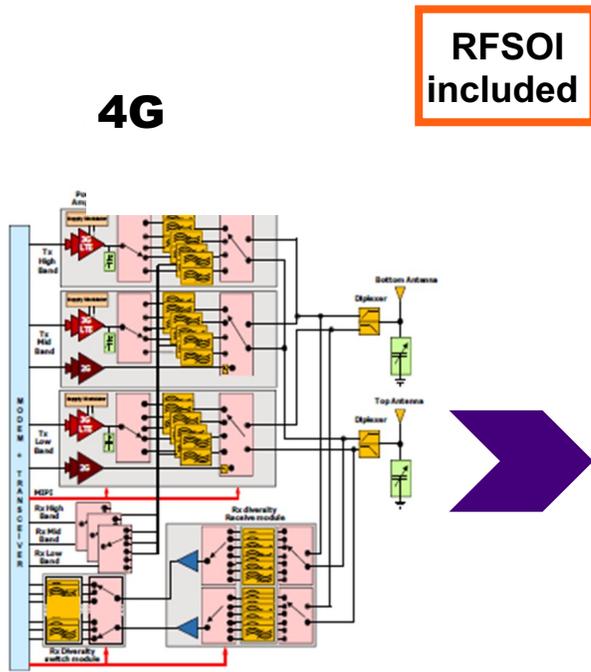
There are 13 antenna RFSOI antenna tuners in the iPhone 14 ! (20mm² of RFSOI area)

Antenna Efficiency (dB)



Cellular RF Front End architecture evolution

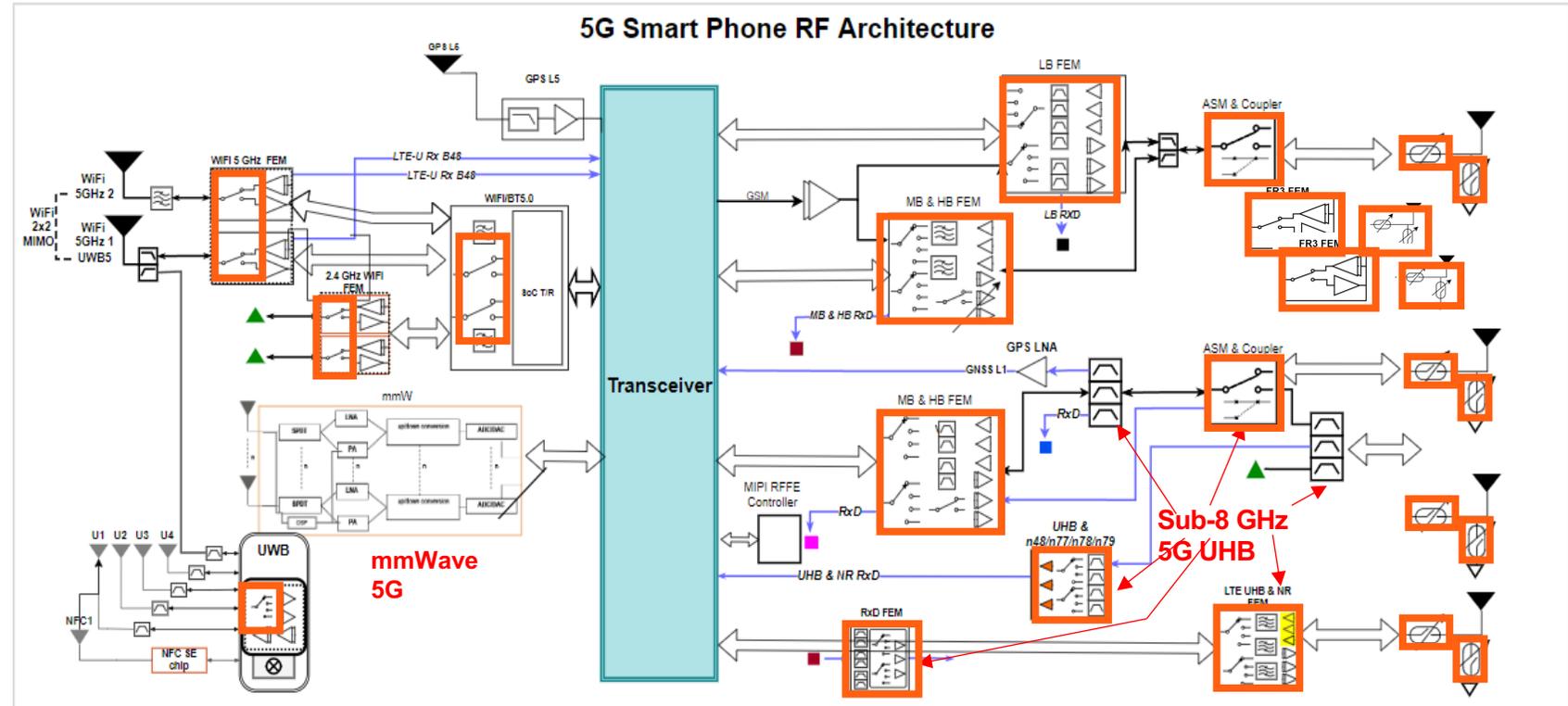
- Increased RFSOI content due to the complexity of 5G mobile handsets



Source: Soitec

- Max #bands: 25
- Max #antenna: 4
- Carrier aggregation & 4x4 MIMO
- RFFE Si Area: 30-40 mm²

RFSOI included



- Max #bands: >40
- Max # Antenna: >8
- 4G-5G coexistence and higher frequency bands : Stringent SW loss, isolation, linearity, LNA performance
- RFFE Si area: >80 mm²

6G will have more #bands, higher carrier frequencies – need for technology differentiation for performance and battery power

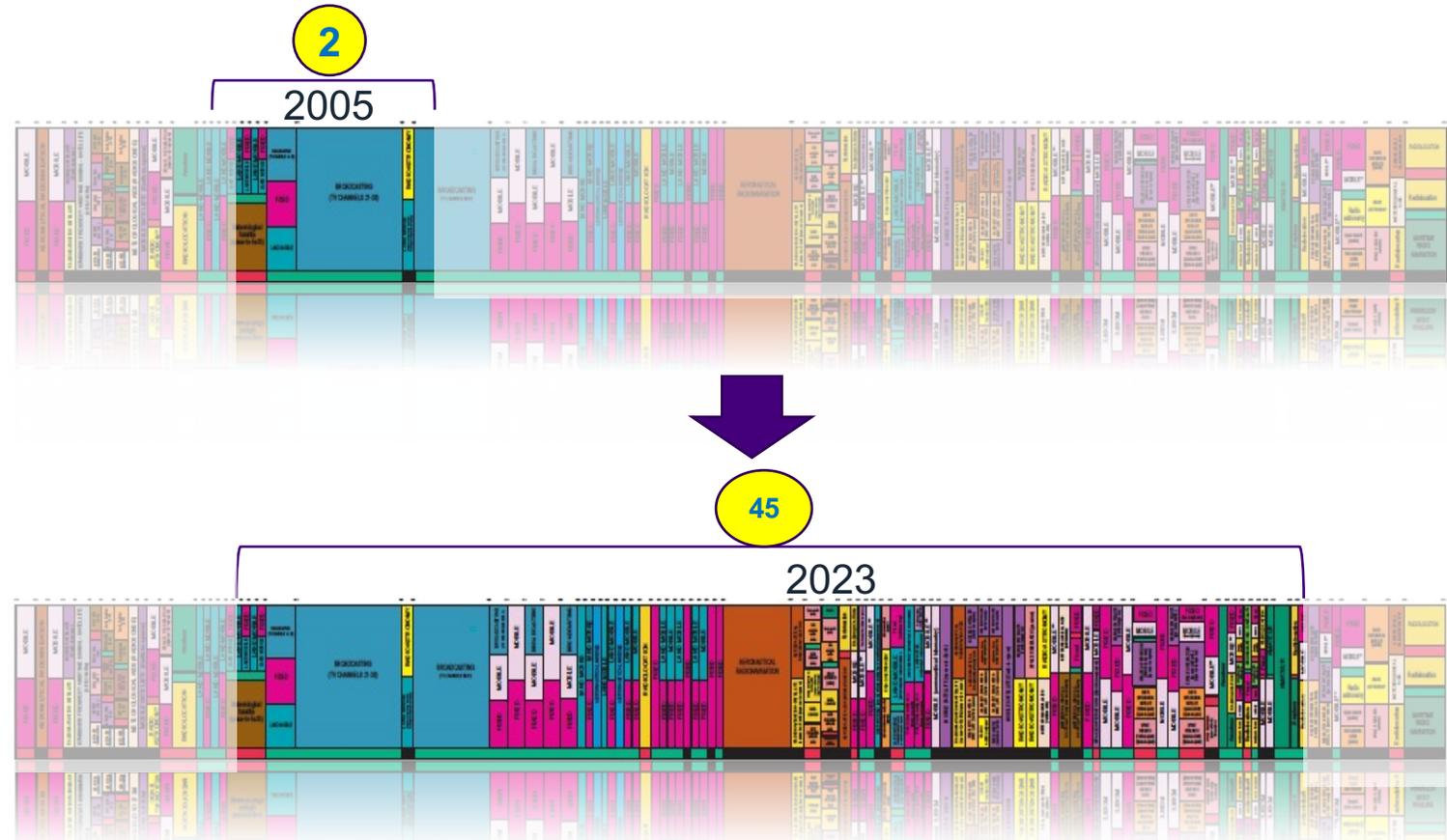
How many cellular bands need to be supported in a premier tier 5G phone today (2023)?

• A. 10

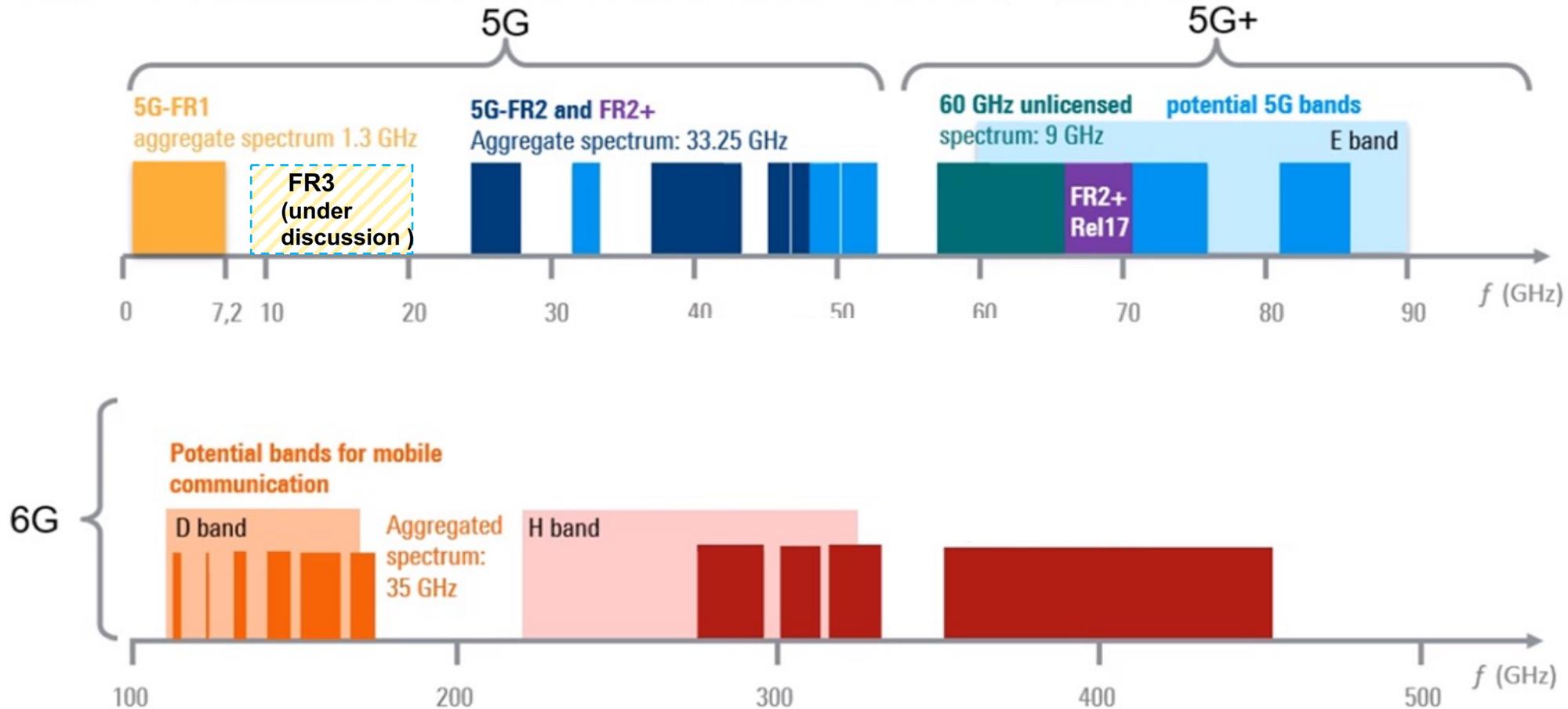
• B. 20

• C. 30

D. 45



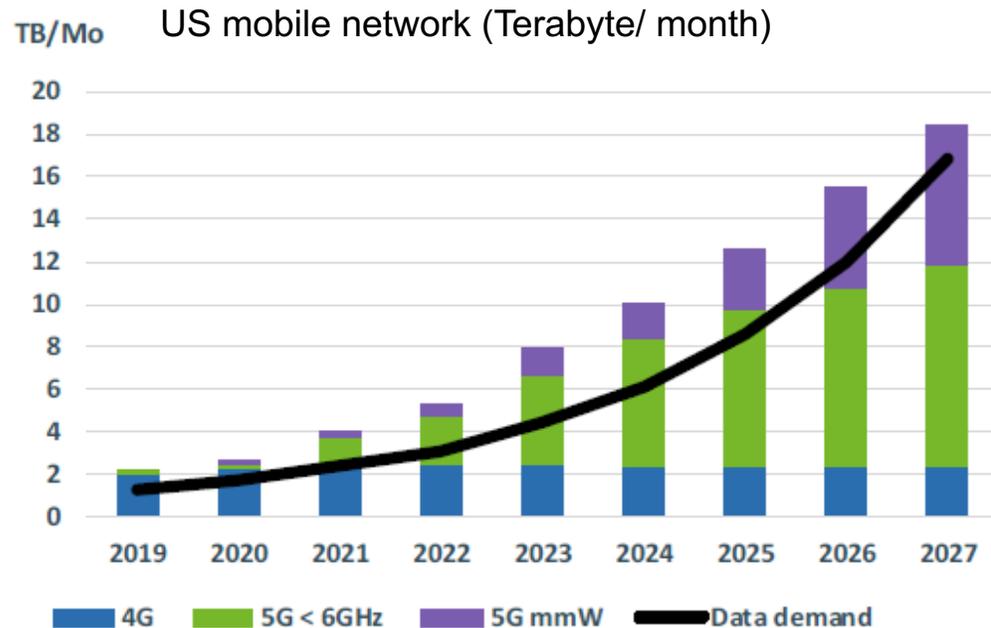
Congested licensed bands below 6GHz – motivation for higher carrier frequencies



Higher Frequency band --> Higher contiguous spectrum bandwidth --> Higher data rate

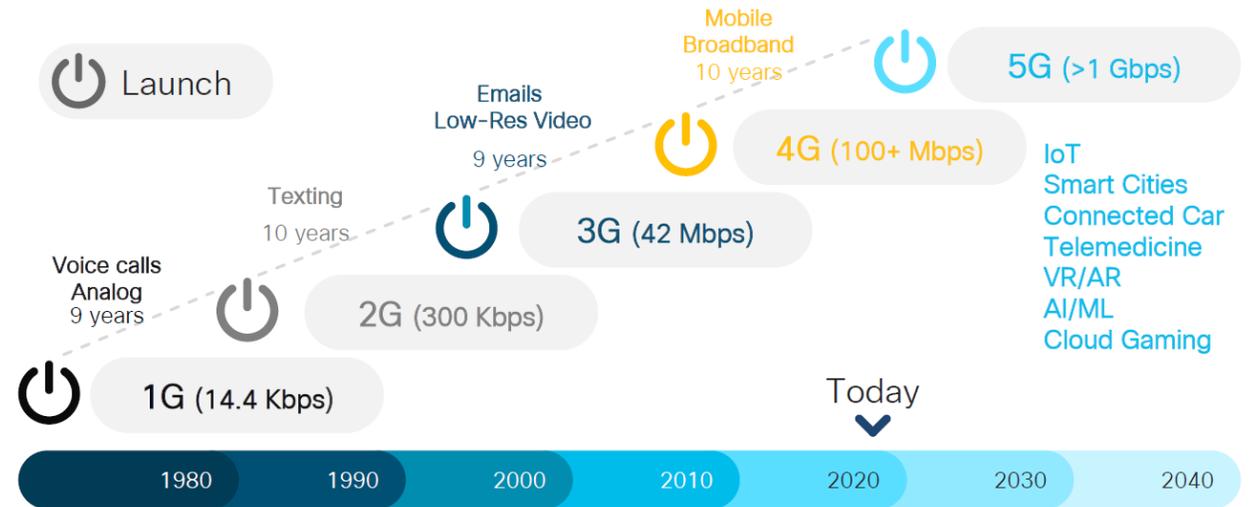
Revolution of mobile communication technology

- Mobile data volume and speed to increase >10X in 10 years.



Mobile Speeds and Technology Evolution

New technology generations occur around every decade with more capabilities



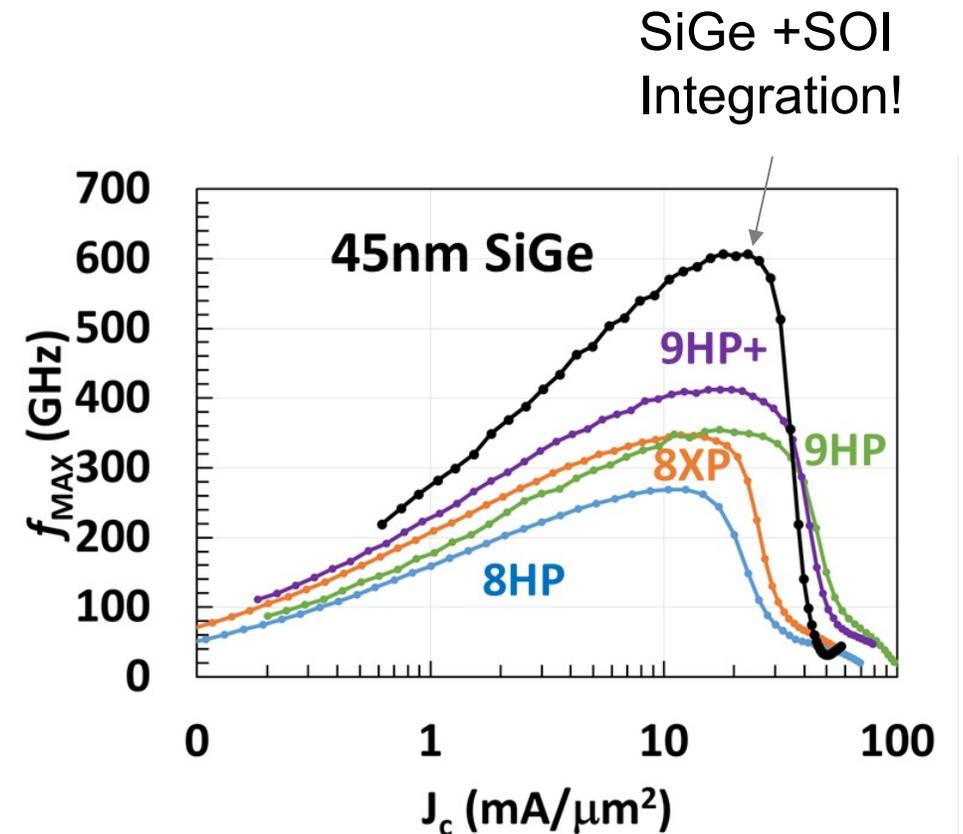
Source: <https://www.eetimes.eu/rf-soi-engineered-substrates-at-the-heart-of-modern-rf-mmwave-front-ends>

Source: Cisco Annual Internet Report, 2018–2023

45nm RF-SOI SiGe BiCMOS Development



- First RFSOI-based BiCMOS demonstration with SiGe NPN HBTs having f_T/f_{MAX} 388/600 GHz.
- 45nm SOI CMOS digital & RF FET baseline process
- High resistivity SOI substrate and high-Q passives
- Combines best of SOI and HBT for >100GHz phased arrays
 - SOI NFET for superior LNA, switch, phase shifters, passive mixer
 - SiGe HBT for higher PA Pout & PAE and lower phase noise VCO



Where are we headed next in RFSOI?

- 3D System Integration will apply to RFICs for dramatic footprint reduction (IMEC's vision)
- RF components must however simultaneously manage: RF coupling / distortion / heat dissipation

Vision and Grand challenges 3D System Integration

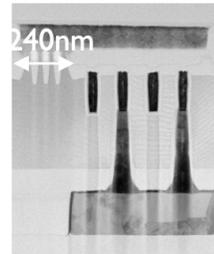
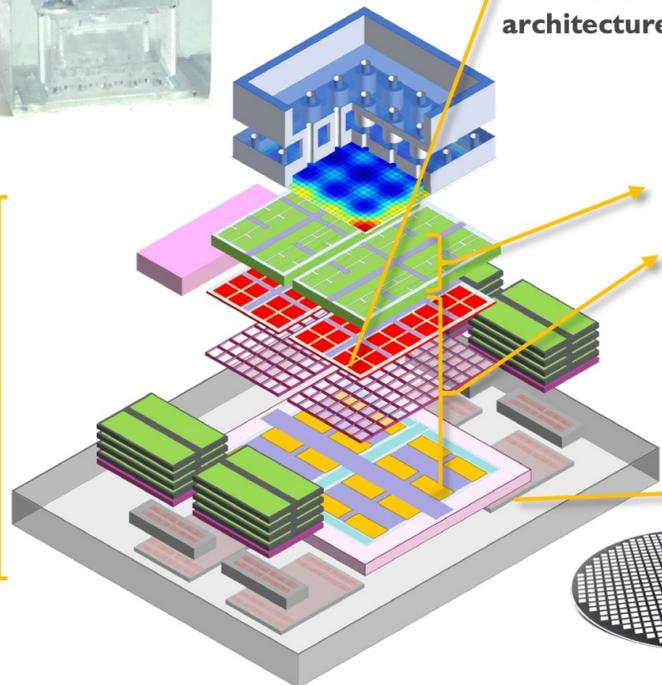
3D2 - High Performance cooling for 3D
Heat spreading & heat removal



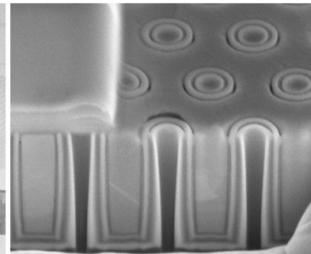
3D5 - Improved Power delivery network architectures

3D2 - Mechanical modelling and characterization

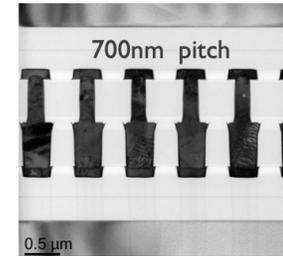
3D1 - Design for 3D SOC
3D high bandwidth interconnects;
3D Power delivery solution
PPAC analysis



BPR/nTSV



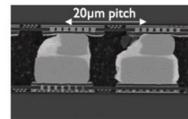
2.5D MIMcap



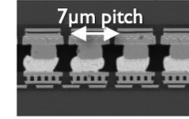
3D4: High Density W2W Stacking: Pitch = 700nm \Rightarrow 500nm \Rightarrow 400nm

3D3: High Density D2W Stacking

SCALED μ BUMPS
Pitch 40 \Rightarrow 20 μ m



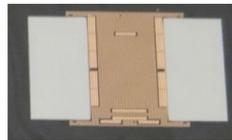
EMBEDDED μ BUMPS
 \Rightarrow 10 \Rightarrow 5 μ m



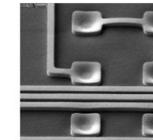
CU/CU DIRECT BONDING
 \Rightarrow 5 \Rightarrow 2 μ m



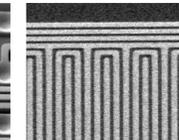
3D6: High density reconstructed wafer interposer, fine pitch RDL



Si Bridge in FO-WLP



2 μ m L/S semi-additive RDL

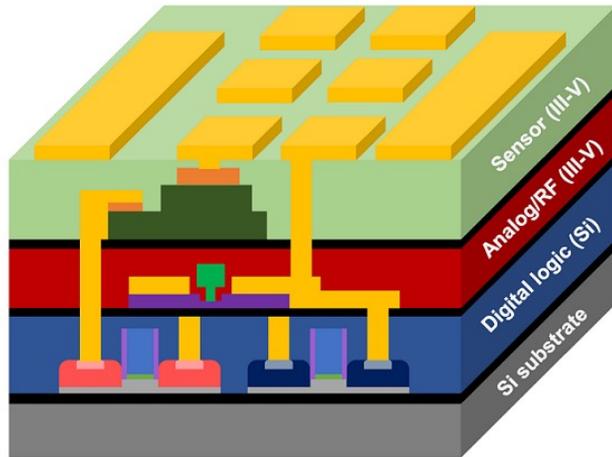


1 μ m L/S Damascene RDL

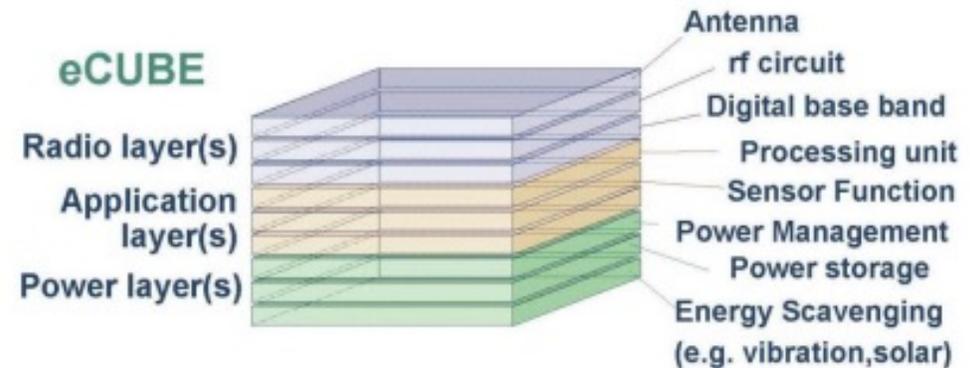


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3D Heterogeneous Microsystems are multi-layered structures that integrate different materials and components in a compact and vertically stacked fashion



3D-system in package (SiP) concept for the realization of fully autonomous systems

Conclusion

- Dramatic increase in mobile data traffic in next decade
- RFSOI-on-HRSI technology readily established in all major cellular 4G/5G platforms
- Substrate treatment technologies closed the gap in performance. Best tradeoff in cost/size/technology compared with other technologies.
- Rapid deployment of RFSOI multi-throw switches and capacitor arrays/tuner products for next generation wireless applications
- RF handset solutions will utilize a number of technologies to dramatically decrease component footprint