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Global Family,
Global Solutions!

A Dive Into Various Wafer Types for RF Optimal Performance

Bruno Baccus

26/04/2024

Incize 10-year Anniversary Event

RF Applications and Link to Wafer Options

- RF space offers interesting connections between the initial condition (wafers) and the final application
- Wafer characteristics -> RF performance (ex: high frequency, harmonics) –> System integration -> final device (ex: 5G smartphone)
- This is why the initial wafer material, design and characteristics are of specific importance besides usual requirements (doping, flatness…)

RF semiconductor materials

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Material	Advantages	Applications
Silicon (SI) **CZ** **FZ** **SOI**	Low cost & Ease of fabrication : Si is abundant and cost-effective Si-based devices can be manufactured using mature CMOS technology. Integration: Si allows integration of digital and analog circuits on a single chip	RF switches Low-power RF applications IoT devices Consumer electronics High Frequency CMOS Even higher frequency with SiGe HBT integrated with CMOS
Gallium Nitride (GaN)	Wide bandgap: GaN has a larger bandgap than GaAs, allowing it to operate at higher temperatures. High breakdown voltage: GaN devices can handle high voltages High electron mobility: GaN transistors are used in power amplifiers for wireless communication	RF power amplifiers (especially in 5G networks) Radar systems Satellite communication Base stations
Gallium Arsenide (GaAs)	High electron mobility: GaAs exhibits excellent electron transport properties, making it suitable for high-frequency applications Low noise figure: GaAs-based devices are commonly used in low-noise amplifiers (LNAs) for sensitive RF receivers High power handling capability: GaAs power amplifiers are prevalent in RF communication systems.	RF filters LNAs Power amplifiers Switches Phase shifters Oscillators Antenna tuners
LT and LN wafer substrate: LiTaO3 (Lithium Tantalate, LT) and LiNbO3 (Lithium Niobate, LN)	Multi-function crystal material which possess unique optical, piezoelectric and pyroelectric properties LT and LN are widely applicable in wireless communication field	Wi-Fi, 4G, 5G, GPS and also use on device for high speed fiber-optic communication
Silicon Carbide (SiC) **Semi-Insulating SiC** **GaN on SI-SiC**	High-temperature operation: SiC devices can withstand extreme temperatures.	High-power RF amplifiers
	High breakdown voltage: SiC is used in high-power applications.	Harsh environment applications (e.g., aerospace, automotive)
	Excellent thermal conductivity: SiC dissipates heat efficiently.	Wireless power transfer

SAS Strategic Layout of Key Areas

Sino-American Silicon Products Inc.

GlobalWafers
Semiconductor Wafer (Incl. Compound semiconductor)
- Key substrate for semiconductor components
- Power management, automotive, communication, MEMS

AWSC
GaAs Foundry
- Penetrate Compound semiconductor market
- RF, 5G, Wifi6, EV, Satellite

Ancora
GaN Power Semiconductor
- GaN tech and solution
- Consuming products, communicate
- and automotive electronics

Transphorm
GaN Power Conversion Products
- Highest reliability GaN devices for high voltage power conversion applications
- Power supplies, RF, Automotive, 5G

Billion
Energy Storage
- Energy storage system integration

Energy storage system installation and EMS development

SES
Energy trading
- Providing Comprehensive Green Energy Solutions
- Planning and developing multiple renewable energies, aligning needs between buyers and sellers

Actron
Automotive
- Seize EV/HEV trends
- EV/HEV, ABS, ADAS, Powertrain

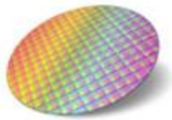
Crystalwise
GaAs, LT, LN
- Key substrate for numerous components
- Optoelectronics, semiconductor, optical fiber communications, wireless communications

ANJET
SiC & GaN Power Semiconductor
- SiC, GaN tech and solution
- EV、Green Energy

TSC
Specialty Gas
- Credible supplier of specialty gas for advanced semiconductor process
- Disilane, Trisilane

NextDrive
Internet of Energy Service
- Via IoT to integrate energy tech
- Energy gateway, cloud computing, device data management

GWC has the world largest wafer product portfolio



	Wafer Diameter (mm)			End-applications
	LE150	200	300	
Annealed Wafer		✓	✓	Memory, LCD Driver, Analog/Logic IC
EPI Wafer (Epitaxial)	✓	✓	✓	Power Device, Automobile, MPU/MCU, CMOS Image Sensor
Polished Wafer	✓	✓	✓	Communication, Power Device, Analog/Logic IC, Memory
Diffused Wafer	✓			Automobile, Electricity, Aerospace
Non-polished Wafer	✓			Discrete Device
FZ Wafer (Float Zone)	✓	✓		Medical Equipment, Wind Turbine, High Speed Rail, Automobile
SOI Wafer (Silicon on Insulator)	✓	✓	✓	High Voltage Power, MEMS Sensor, CMOS, RF Device, Photonics
SiC Wafer (Silicon Carbide)	✓	✓		Automobile, High Voltage Power, High Speed Rail, Wind Turbine
GaN/Si, GaN/SiC (Gallium Nitride)	✓	✓		Solar Inverter, Power Supplies, RF Power

Polished Wafers – CZ Silicon

- (100) lightly doped wafers
  - 10's-100's ohm-cm for SiGe technology
  - >1000 ohm-cm for passives (high-Q inductors)
- CZ Crystal Growth
- Less demanding design rules / wafer parameters

	150mm	200mm	300mm
Diameter	✓	✓	✓

Positive	Cost	Availability

Negative	Thermal Donors	Extra Design

Example Impacts of Resistivity

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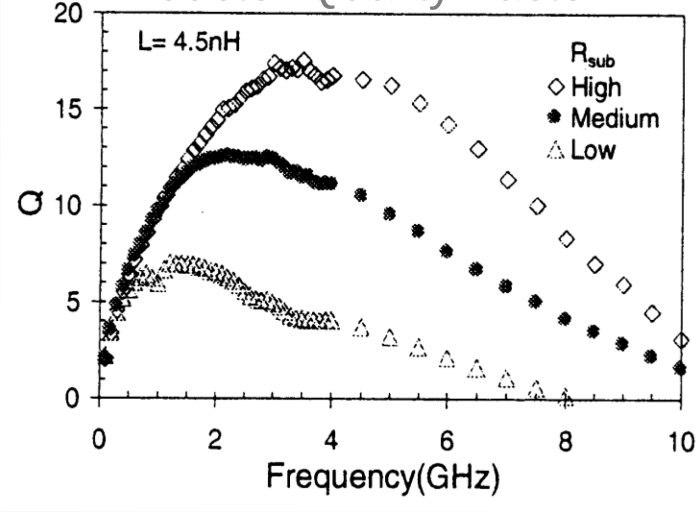
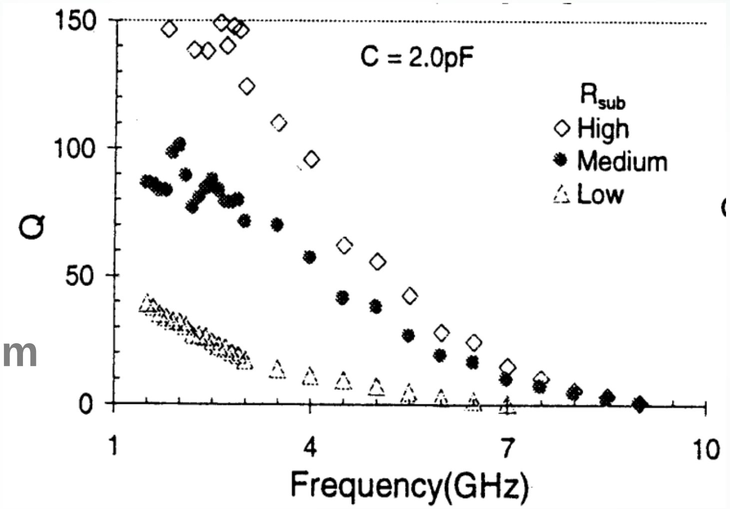
Inductor Quality Factor

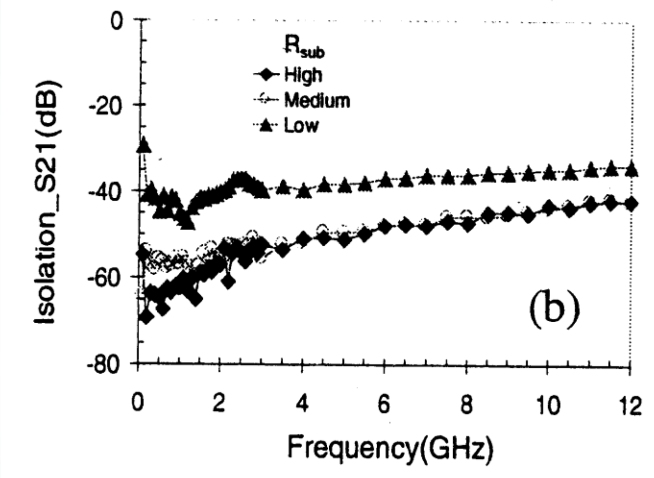


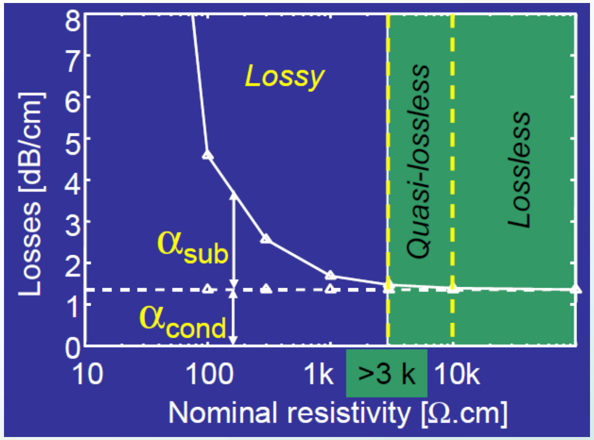


High>1000Ωcm
Medium~20-60Ωcm
Low<5Ωcm

Yang, et al,
IEDM2002, 27.8,
pg 667-670.

Cross-talk isolation





J.P. Raskin, IEEE
S3S Conf. 2013

High RF and THz – Si-based

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IEDM 2022, Paper 11.7 (ST Microelectronics):

- 130nm bulk HiRes SiGe BiCMOS (ft 230GHz / fmax 280GHz) with low Ron-Coff and high power handling for WiFi 6E RF front end module.
- Complementary to RFSOI w/intent is to offer non-SOI RF FEM for cost sensitive 6G applications while improving power efficiency and better noise figure.
- RFSOI supports WiFi FEM to 2.5GHz, but SiGe enables WiFi FEM to 6GHz.
- Evaluated 1kohm-cm vs 125ohm-cm substrates and prefer 125ohm-cm as more practical and good enough, less prone to latch-up, and easier to acquire with fewer use challenges.
- Higher parasitic capacitance than SOI (absence of BOX) limits power handling. “RFSOI is king for high end front end module”

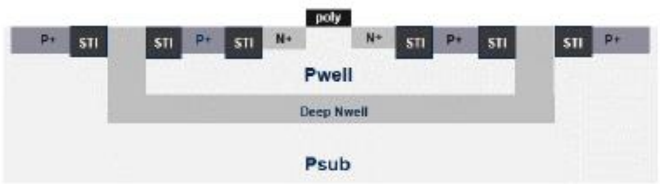

Fig. 1. Triple well device architecture

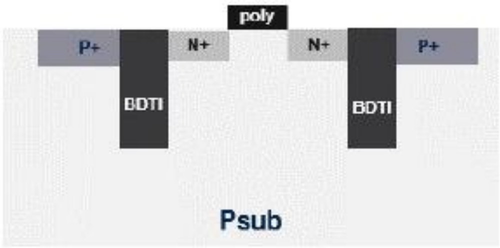

Fig. 2. DTI isolated NMOS architecture

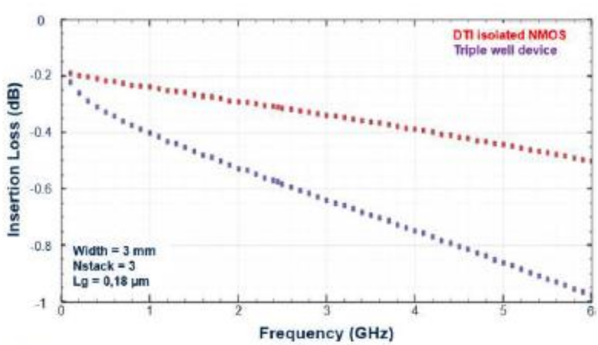

Fig. 3. Comparison of insertion loss of triple well vs DTI isolated NMOS

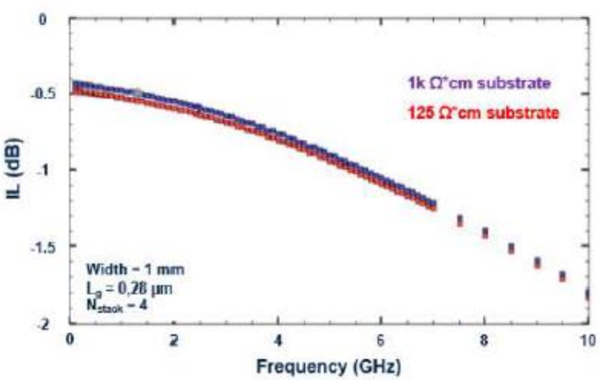

Fig. 4. Substrate resistivity impact on achieavable insertion loss

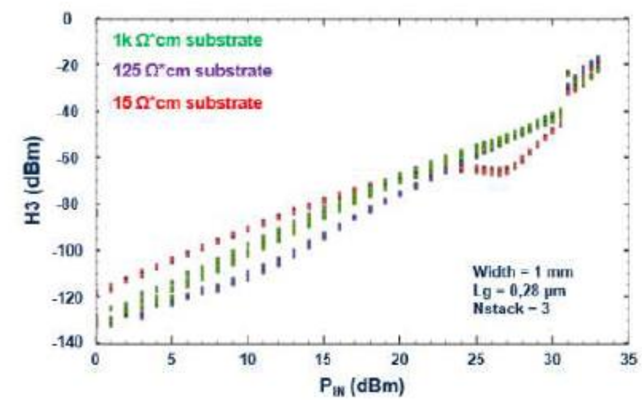

Fig. 5. Substrate resistivity impact on achieavable 3rd harmonics in OFF state

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Polished Wafers – FZ Silicon

- (100) or (111) highly doped wafers (>1k ohm.cm, Max 50k ohm.cm)
- FZ Crystal Growth

Growth method	HiRes™ Float Zone Silicon
Resistivity	>1 kΩcm (max resistivity 50 kΩcm)
Resistivity tolerance	±30 - ±50%
Radial resistivity variation	<50 - <60%
Diameter	150-200 mm
Crystal orientation	<100>, <111>*
Type and Dopant	N, P: Undoped
Oxygen and Carbon concentration	$<10^{16}$ cm^{-3}
Wafer thickness	>200-1300 µm depending on wafer diameter
Wafer surface finish	Single side polished and double side polished

- GHz & THz applications
- RF MEMS switches
- High-Q inductors and capacitors
- GHz Transmitter and receiver circuits
- GHz mixers
- GHz Power amplifiers
- Low loss microstrip transmission lines and coplanar waveguides
- Micromachined thin Film Bulk Acoustic Resonators (FBAR)

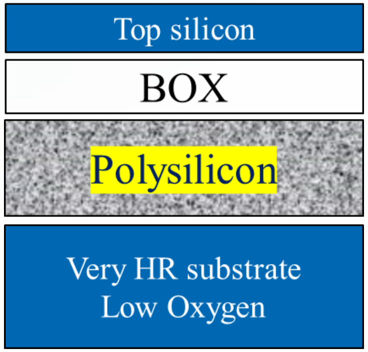
	150mm	200mm	300mm
Diameter	✓	✓	

Positive	Very High Resistivity	

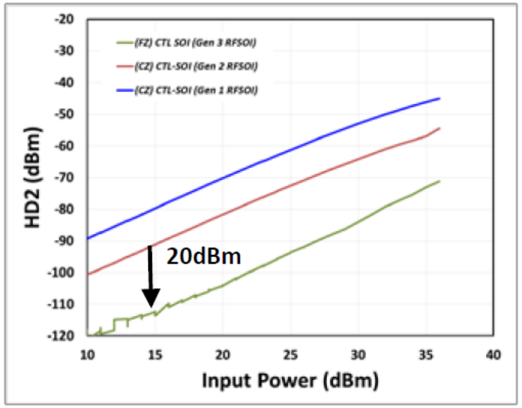
Negative	Cost	Not available on 300mm

SOI for RF

- Hi-Resistivity handles
- CTL – Charge Trap Layer
  - Switches
  - Power Amplifier



Typical RFSOI wafer



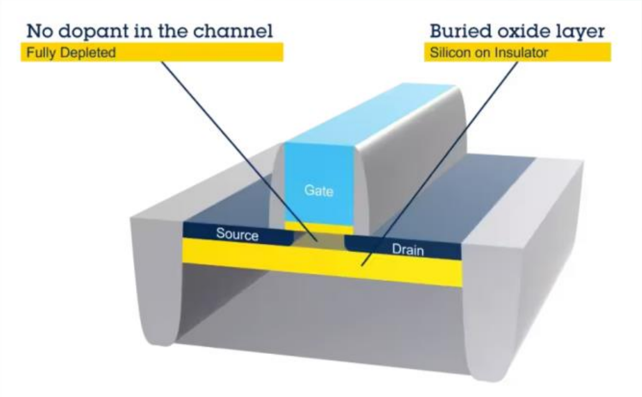
HD2 vs Pin for FZ CTLSOI wafers compared to CZ CTL SOI wafers

	150mm	200mm	300mm
Diameter		✓	✓

Positive	Harmonics Performance	Availability	Top wafer reuse
Negative	Tuning of thermal cycles (Thermal donors, slip lines)	Cost	

SOI for RF - FDSOI

- Very thin Box and Top layers
  - mmWave Front-End
  - SatCom
  - Radar
  - Automotive



Source: ST Microelectronics

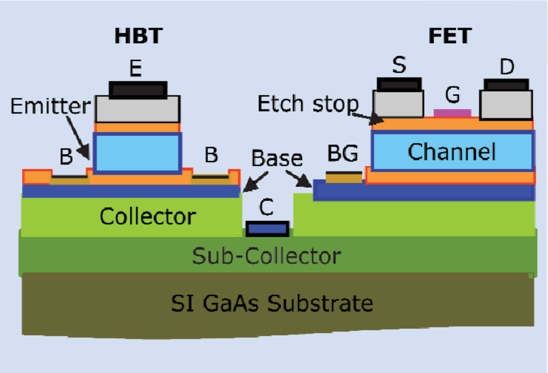
	150mm	200mm	300mm
Diameter			✓

Positive	Digital / Mixed Signal Integration	Back Bias Capability	Low Power Consumption

Negative	Design Complexity ? Challenging wafer specification	Cost

GaAs for RF

- For RF typically bulk GaAs semi-insulating crystal with MOCVD grown III-V epi stack



- There has been research for GaAs on Si

	150mm	200mm	300mm
Diameter	✓		

Positive	Output Power Frequency	Low Noise

Negative	Integration	Cost

GaN for RF

- Si handle – High Resistivity
  (or Semi-Insulating SiC substrate)
- GaN Growth

- GaN on SI-SiC is well established for defense and high temperature applications.

- GaN on HiRes Si(111) is competing in consumer and cost sensitive communication markets

	150mm	200mm	300mm
Diameter	✓	✓	

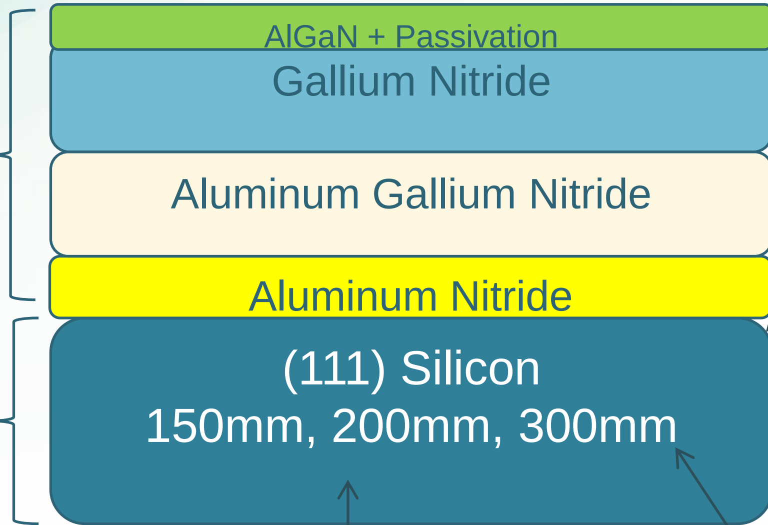
Positive	Output Power	Frequency

Negative	Integration	Cost

GaN Epi on Si(111): Wafer Requirements

MOCVD growth: 150/200mm capability at GWC

Silicon thickness used to offset Stress / Bow from ~ 50% Thermal Expansion Mismatch. 150mm~1mm, 200mm ~ 1.15mm



Edge profile to prevent Ga contact to Si and reduce film cracks, reduce damage from susceptor contact, and for optimum shape after backgrind

(111) orientation for better symmetry match to h-GaN

~ 20% lattice mismatch between Si and GaN…high dislocation density

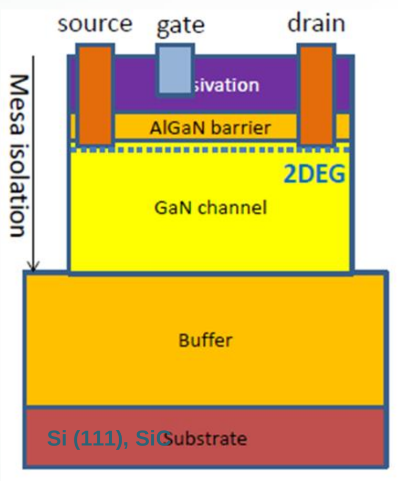
Control of slicing orientation target and tolerance, varies from spec to spec

Increase wafer slip resistance through doping level, oxygen, co-doping with N

P+, P++ for Power GaN provides better shape control

High resistivity > ~3kohm-cm for RF GaN/Si

Semi-insulating SiC for RF GaN/SiC



HEMT = Lateral FET

Power – RF GaN on Si

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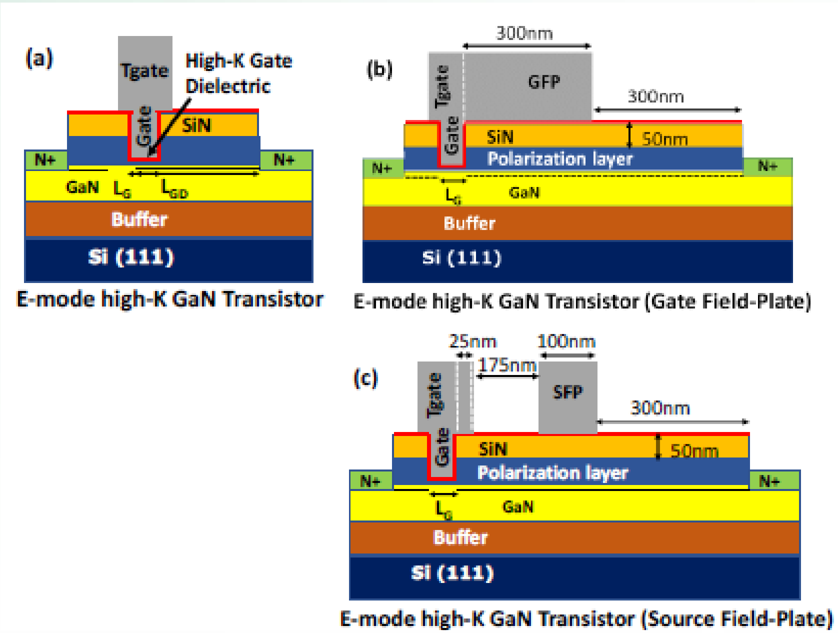
IEDM 2022 Paper 35.1 (Intel): 300mm GaN on Si(111) HRS for high performance RF power. Record high Fmax of 680GHz demonstrated for 30nm channel length enhancement mode transistor. Field plating optimized to extend breakdown voltage and reliability from 12V to 40V range operation. Power FOM (Ron*Qgg) 30X better than Si-LDMOS and 20x better than e-mode p-GaN HEMT.



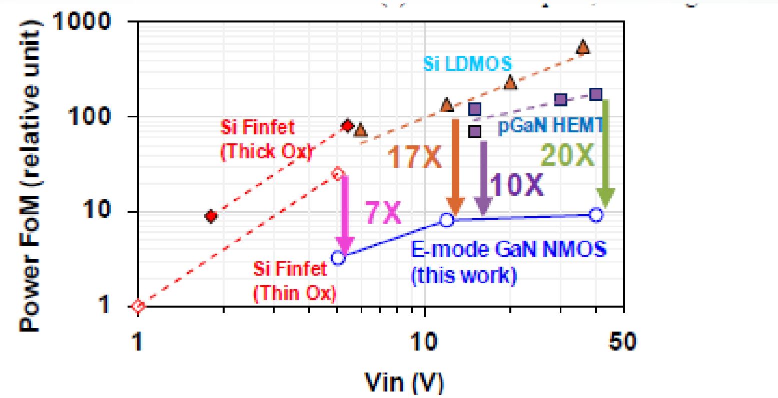


Fig.11 benchmarks the power FoM of the e-mode GaN NMOS of this work, showing ~20X better performance than pGaN HEMT and ~30X better than Si LDMOS at 40V; 10-17X better than Si LDMOS and pGaN HEMT at 12-15V, and 7X better than Si Finfet at 5V.

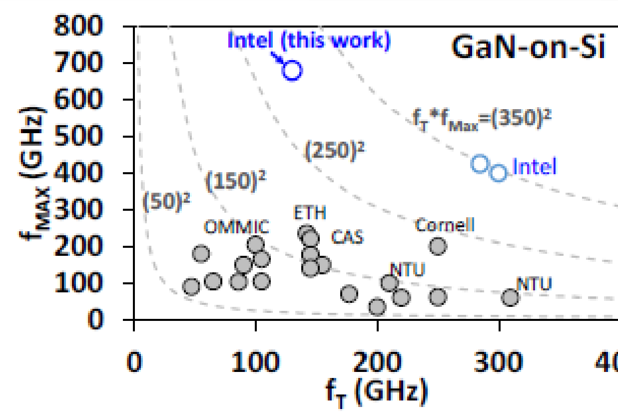


Fig.16 benchmarks the f_T/f_{MAX} of this work with data points reported [13] for GaN-on-Si transistors, showing record f_{MAX}=680GHz with f_T=130GHz, shown in Fig.12. Intel data points are the only ones from 300mm GaN-on-Si(111) process.

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