Characterization of Self-Heating Using Low-Frequency RF Measurements

A.J. Scholten, fellow, NXP Semiconductors

INCIZE 10 years anniversary

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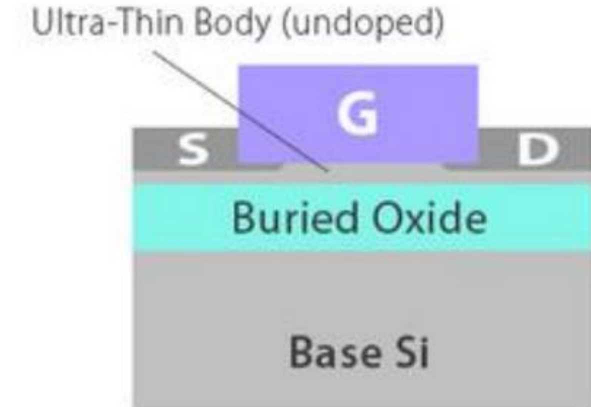
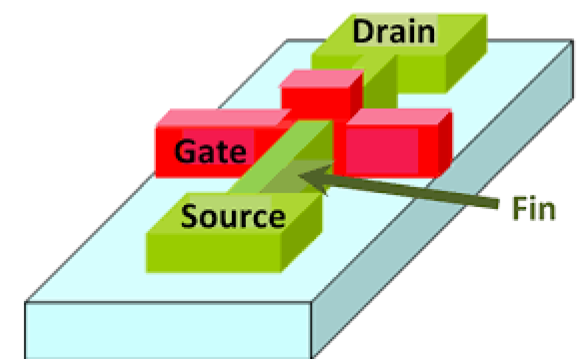
MODENA E REGGIO EMILIA

introduction

- self-heating traditionally topic for LDMOS, SOI devices, bipolar devices
- becoming more important for MOS devices
  - increased power densities
  - 3-D device architectures (FinFET, stacked nanosheets, etc.)



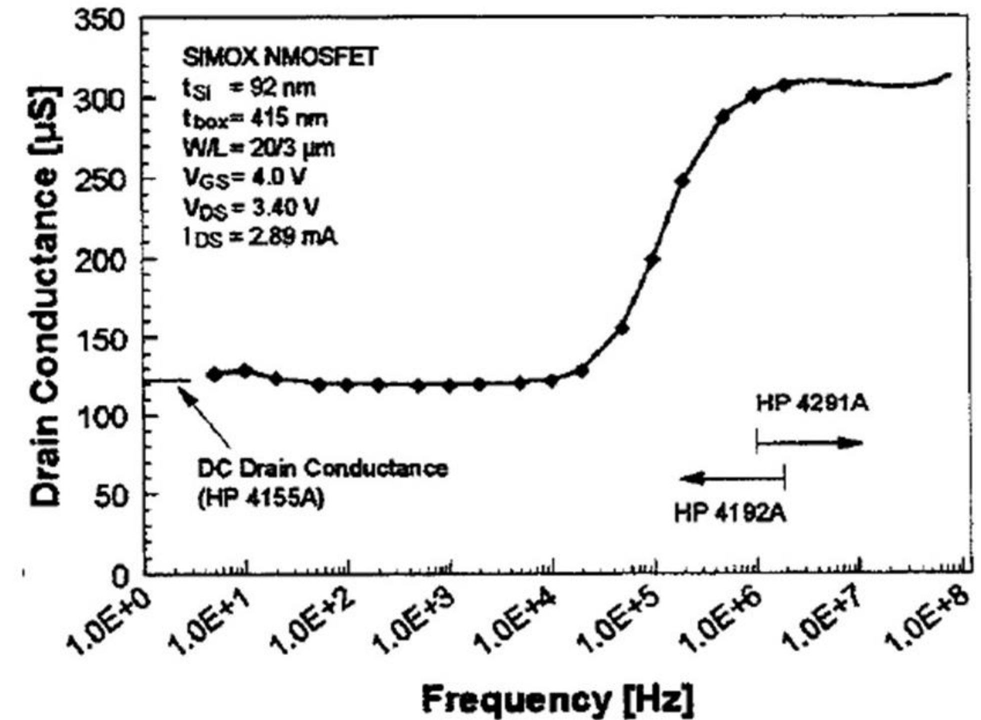
- many methods available for self-heating characterization: pulsed vs DC IV, gate resistance thermometry, optical methods, etc.
- this presentation: AC conductance method*
- also offered by Incize!



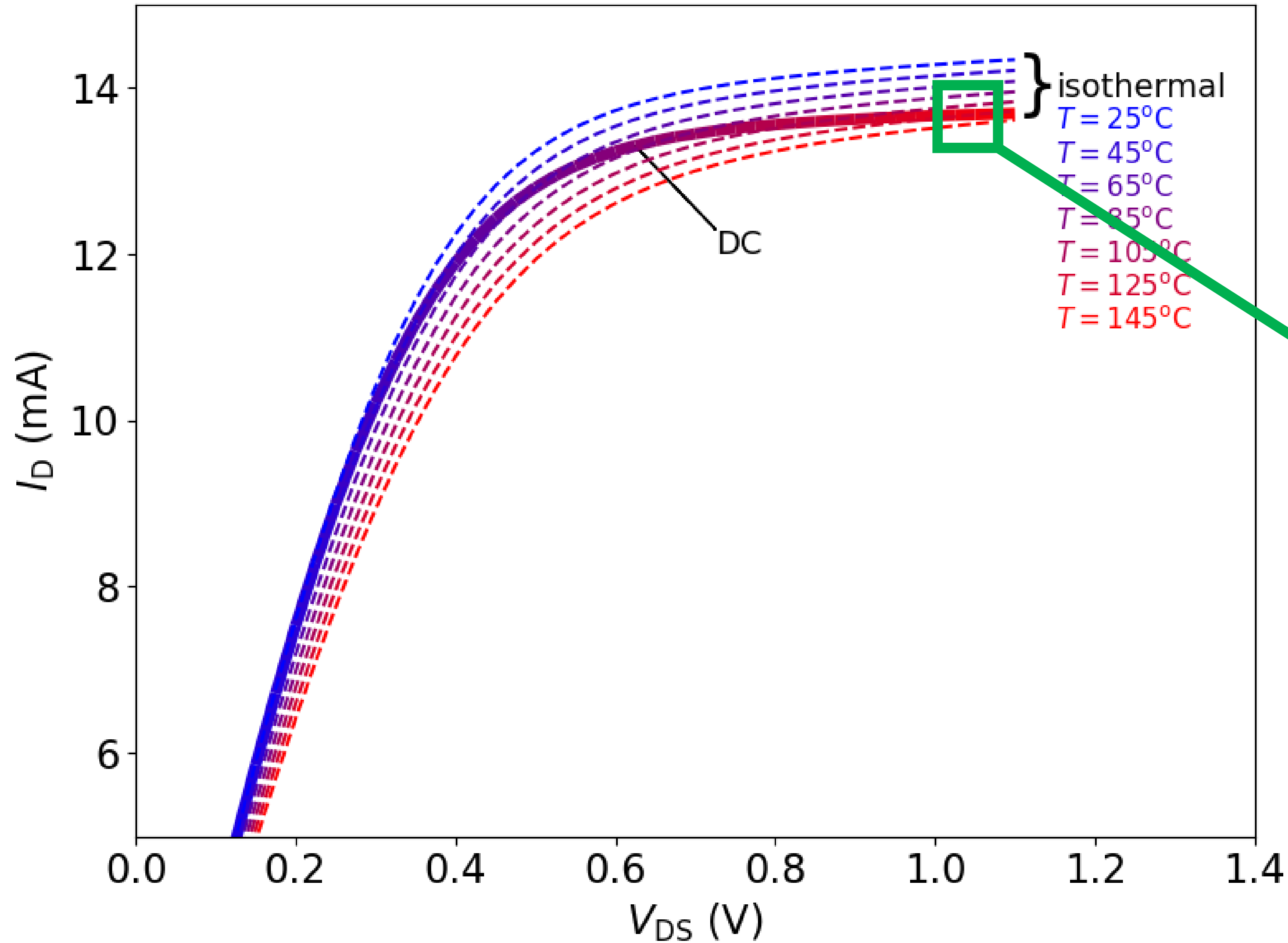
*A. Caviglia and A.A. Iliadis, A New Method for Characterizing Dynamic Self-Heating in SOI Mosfets, 1992 IEEE International SOI Conference, pp. 118-119; W. Redman-White et al., Electronics Letters, Vol. 29, No. 13, p.1180 (1993)

AC conductance method

- relies on dependence of output conductance on frequency due to self-heating
- has been applied to many device types
  - SOI MOSFET: W. Redman-White et al., Electronics Letters, Vol. 29, No. 13, p.1180 (1993); see picture
  - SOI MOSFET: W. Jin et al., IEDM1999, p.175
  - SiGe HBT: S.F. Shams et al, BCTM2002, p. 92
  - GAA Si nanowire: R. Wang et al., IEEE El. Dev. Lett., Vol. 30, No. 5 (2009)



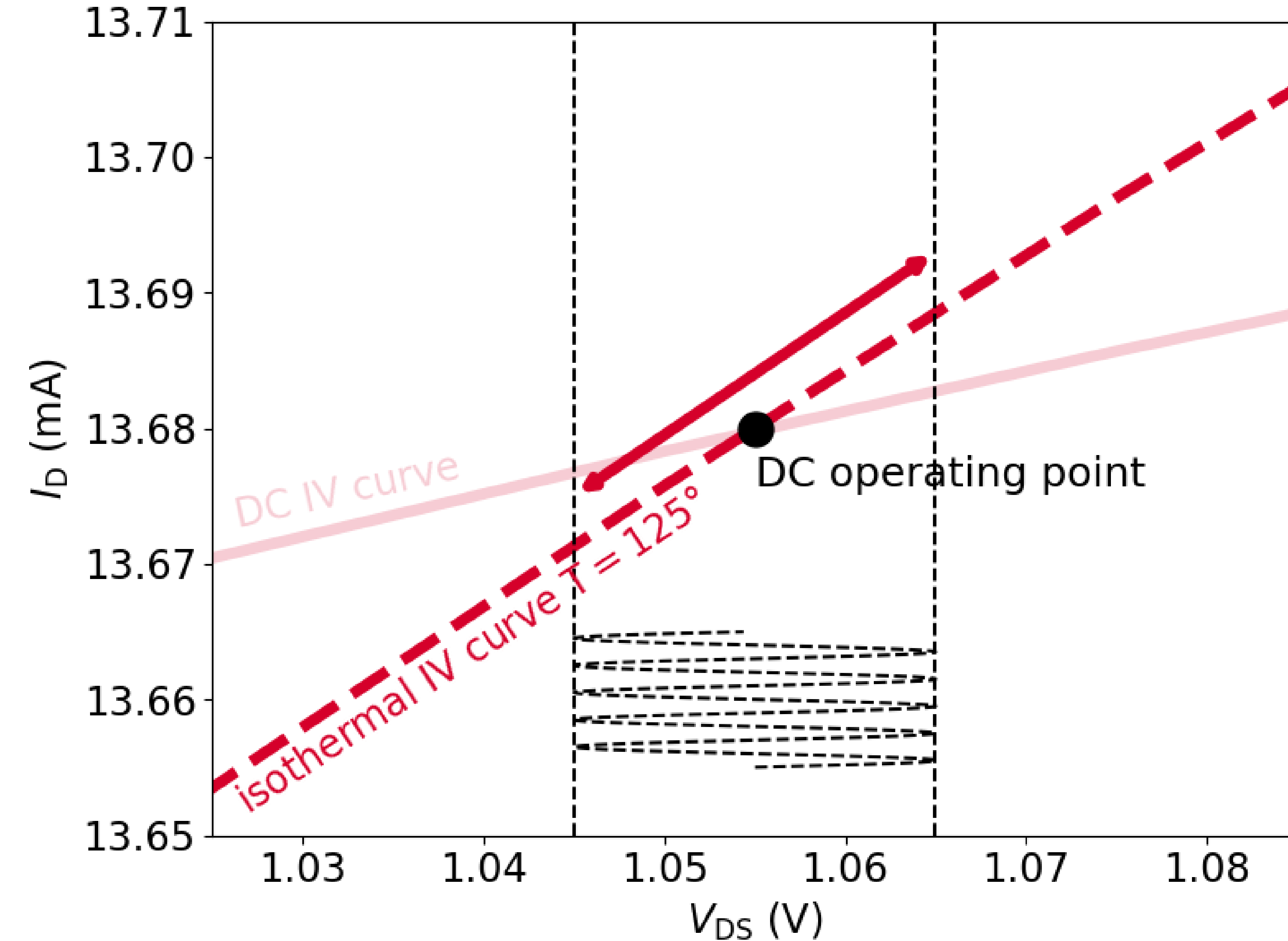
explanation of 'AC conductance method' (i)



the DC IV curve moves from one isothermal line to the next

zoom-in

explanation of 'AC conductance method' (ii)



the DC and isothermal IV curves have different slopes!

for low-frequency AC excitation on the drain, the current response follows the DC IV curve

for high-frequency AC excitation on the drain, the current response follows the isothermal IV curve

with some math, this effect can be used to extract the self-heating ΔT and a full thermal network

but there is more...

- so, the self-heating affects the frequency dependence of **output conductance**
- similarly, self-heating affects the frequency dependence of **transconductance**
- due to delays between power dissipation and actual heating (i.e. thermal capacitance effect), self-heating also affects the **on-state 'capacitances'***
- so, we look at four quantities, derived from Y-parameters:

	quantity	**Formula** (in MOSFET terms)
#1	output conductance	$g_{\mathrm{out}} = \mathrm{Re}\left(Y_{\mathrm{DD}}\right)$
#2	transconductance	$g_{\mathrm{m}} = \mathrm{Re}\left(Y_{\mathrm{DG}}\right)$
#3	output capacitance	$C_{\mathrm{DD}} = \dfrac{\mathrm{Im}\left(Y_{\mathrm{DD}}\right)}{2 \cdot \pi \cdot f}$
#4	transconductance	$C_{\mathrm{DG}} = -\dfrac{\mathrm{Im}\left(Y_{\mathrm{DG}}\right)}{2 \cdot \pi \cdot f}$

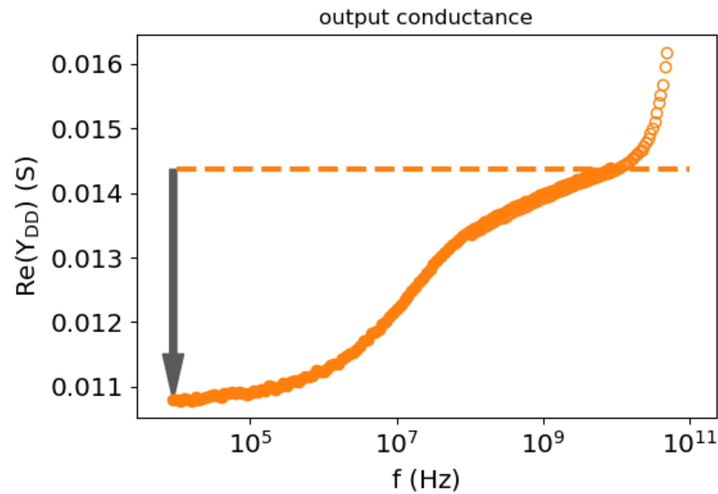
*N. Rinaldi, Small-Signal Operation of Semiconductor Devices Including Self-Heating, with Application to Thermal Characterization and Instability Analysis, IEEE Transactions on Electron Devices, Vol. 48, No. 2, pp. 323–331 (2001); A.J. Scholten et al., Experimental assessment of self-heating in SOI FinFETs, IEDM 2009, pp. 305–308.

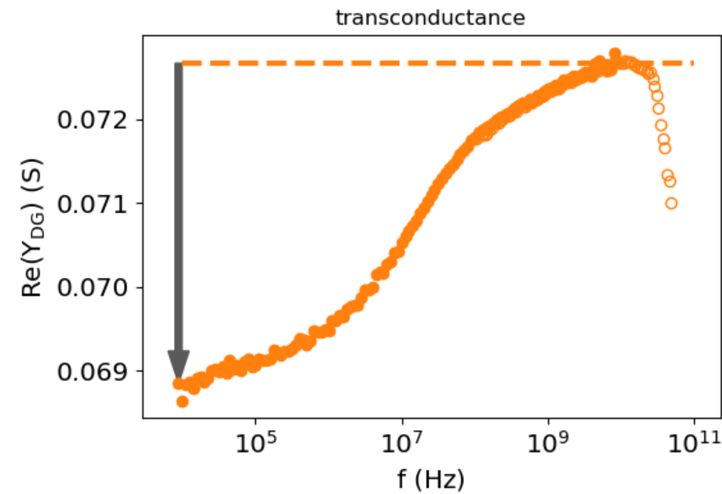
the RF fingerprint of self-heating

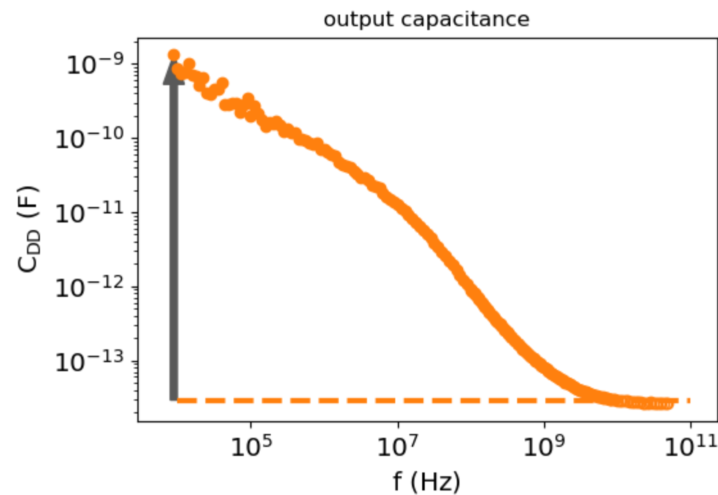
measurement details

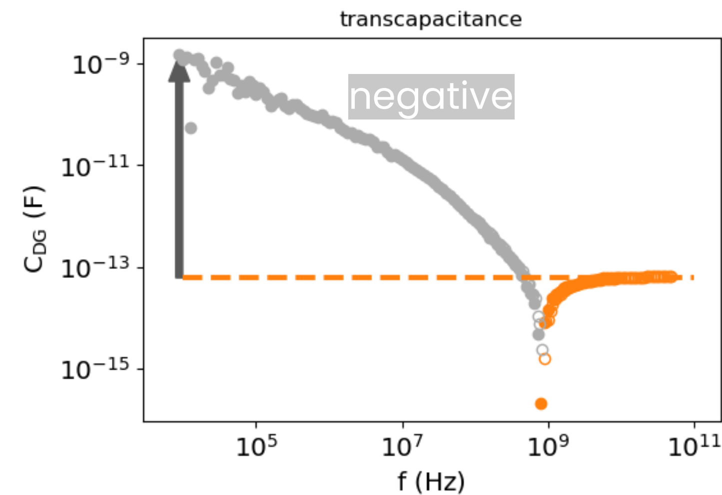
- on-wafer measurements
- standard GSG RF structures
- de-embedding: open-short-load-dedicated open
- analyzers
  - Agilent E5071C ENA (9 kHz – 8 GHz)
  - Keysight N5227B PNA (100 MHz – 50GHz)

N-channel bulk CMOS 32 x 1.5 μm x 30nm; $V_{DS}=V_{GS}=1.0$ V; $dI_D/dT < 0$









at low frequencies:

- output conductance *decreases* (and can even become negative, e.g. for LDMOS)
- transconductance *decreases*
- output capacitance *increases by orders-of-magnitude*
- transcapacitance becomes *negative* and *increases* (in absolute sense) *by orders of magnitude*

N-channel FinFET 4 x 6 x 16nm; $V_{DS}=V_{GS}=1.0$ V; $dI_D/dT < 0$

10 YEARS incize
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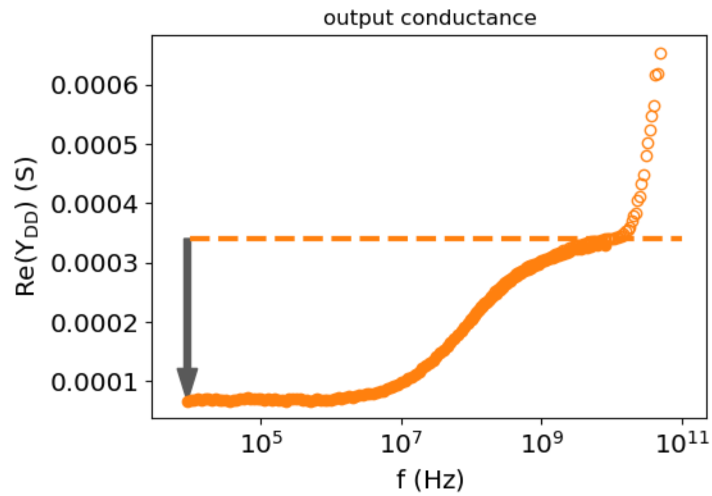
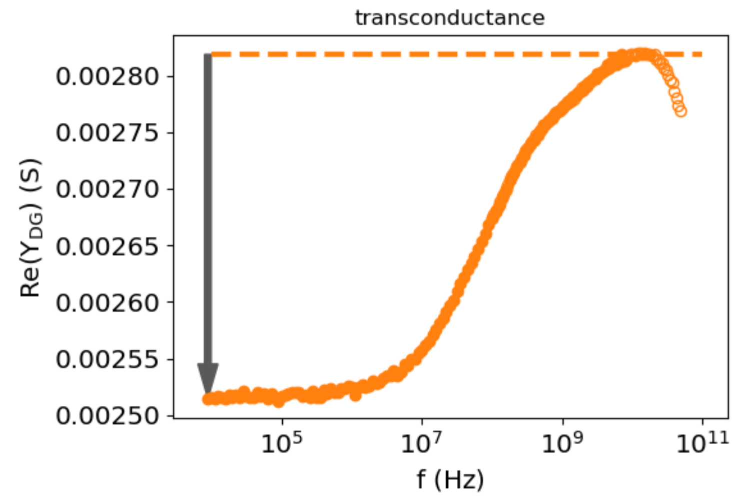
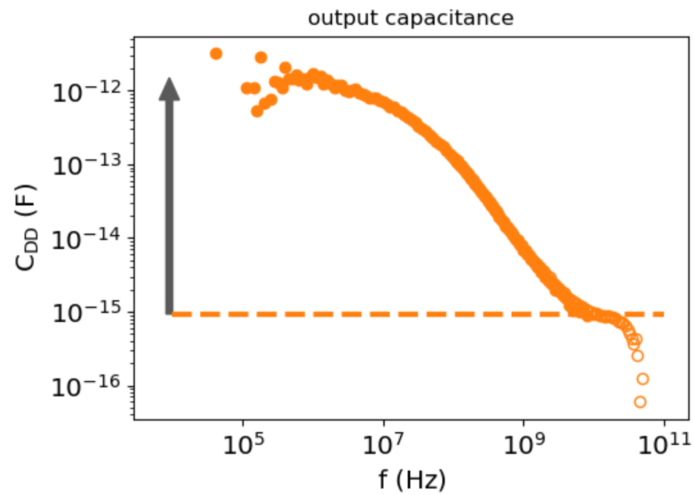
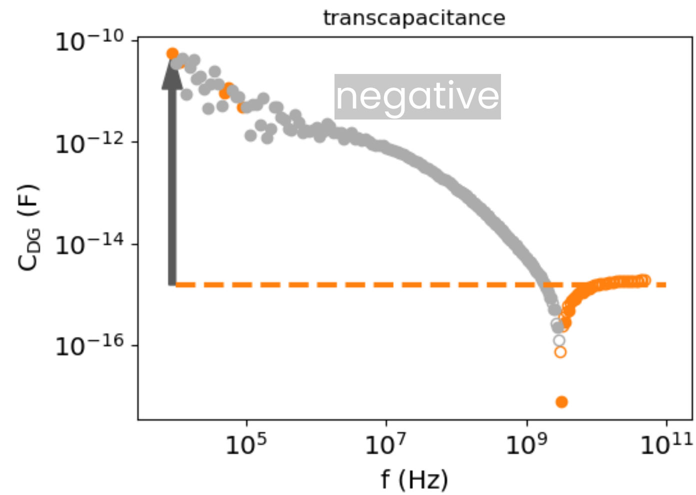
26 APRIL



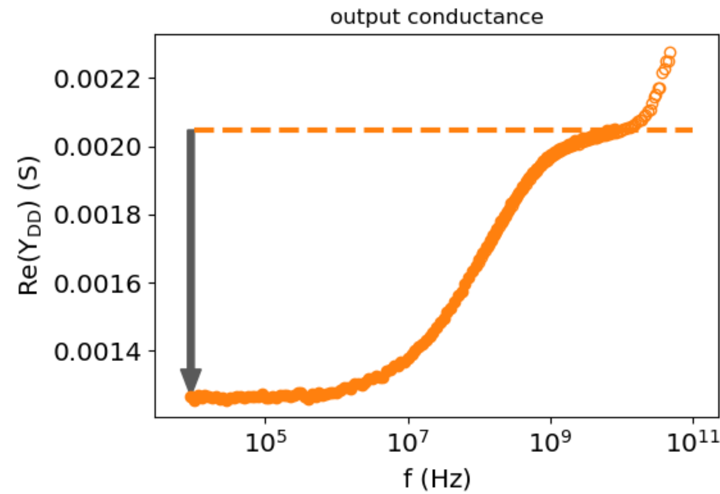


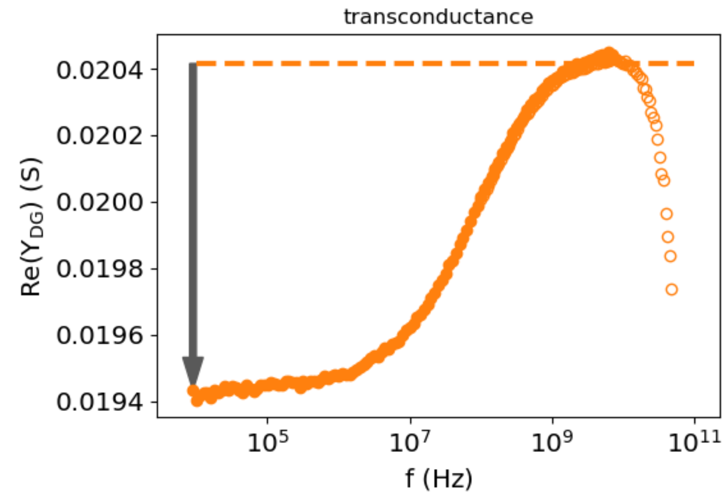


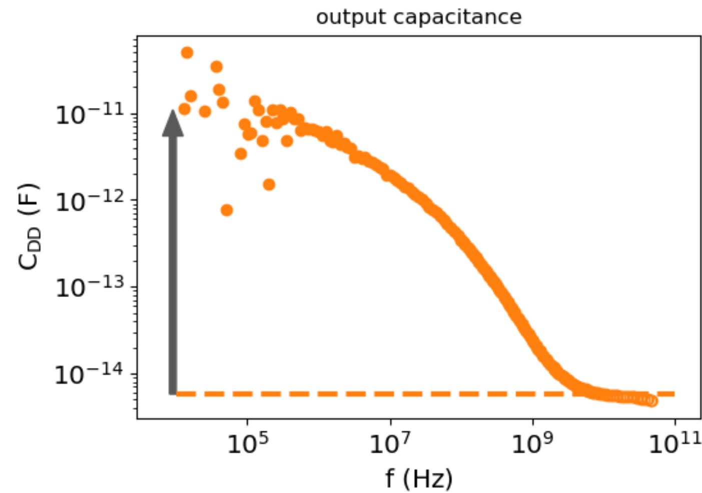


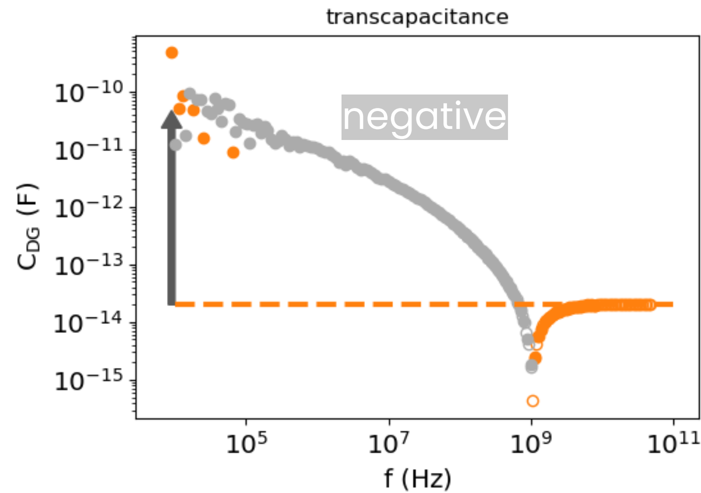
same behavior as bulk CMOS

N-channel FDSOI 32 x 400nm x 20nm; $V_{DS}=V_{GS}=0.8$ V; $dI_D/dT < 0$









same behavior as FiNFET and bulk CMOS

SiGe HBT 0.24 μm x 10.016 μm; V_{BE}=0.8 V; V_{CE}=2.0 V; $dI_C/dT > 0$

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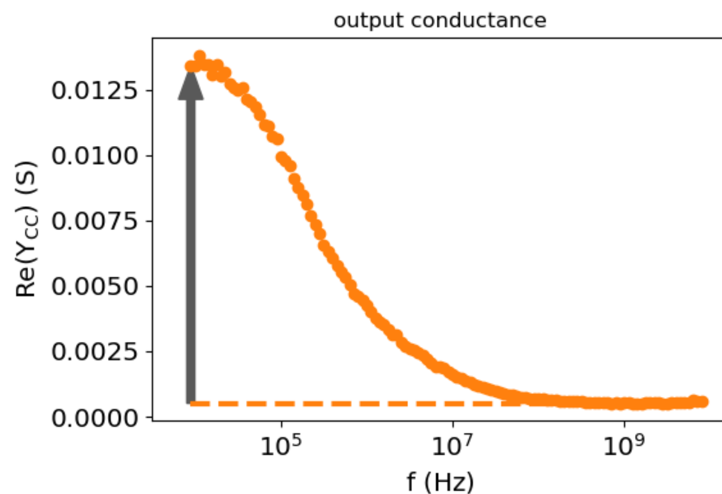

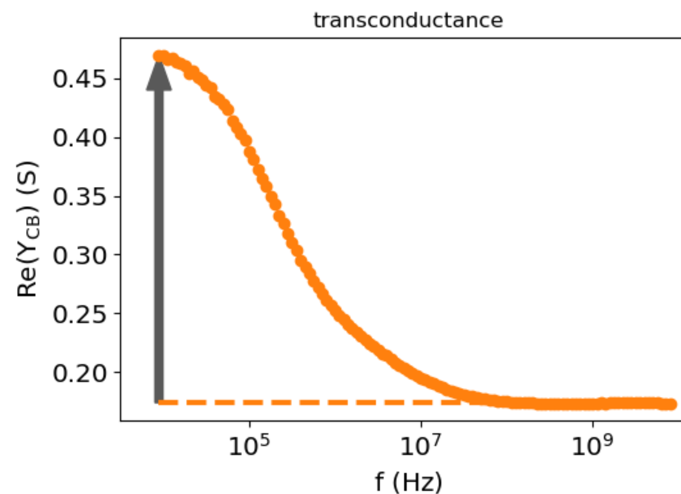

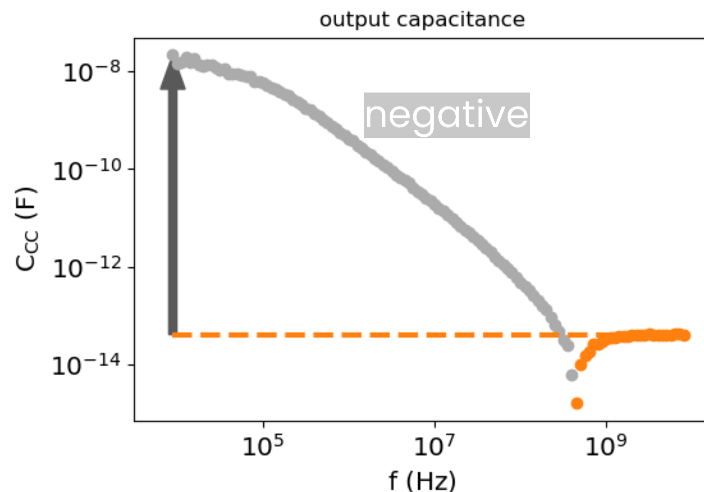

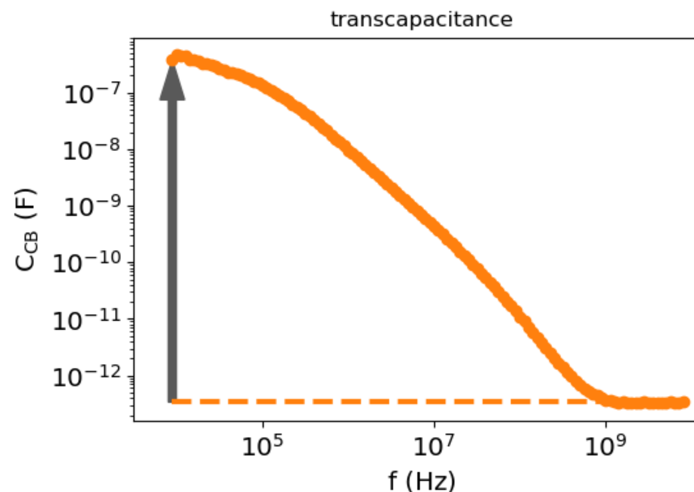

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- transconductance *increases*
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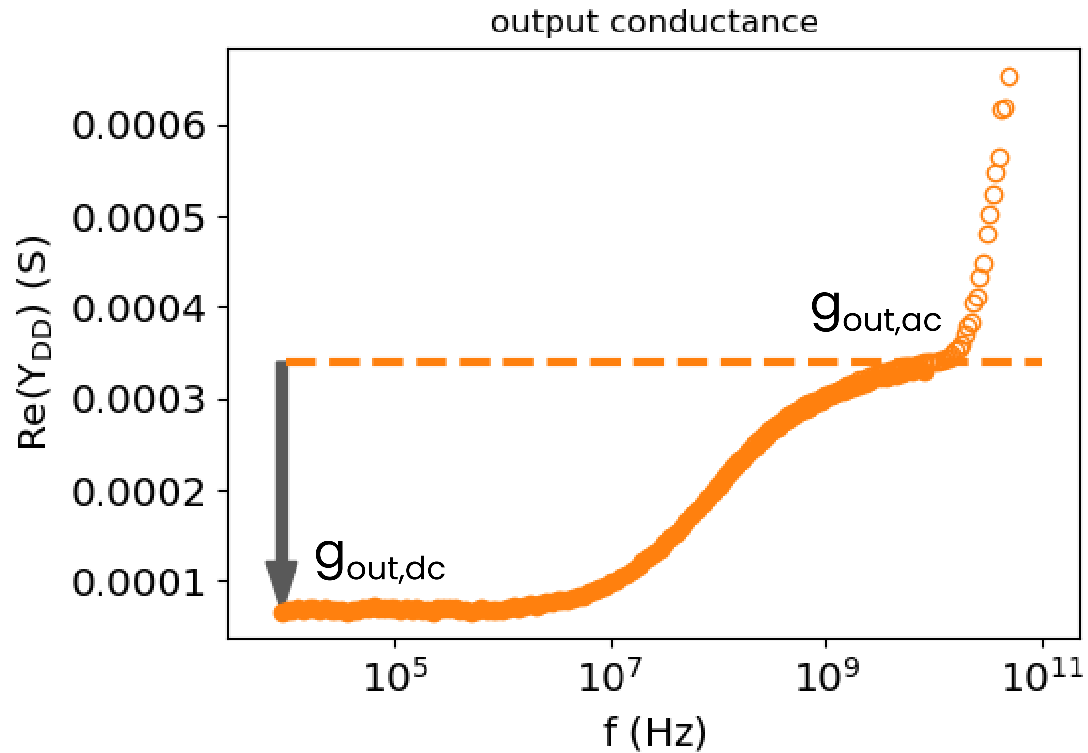
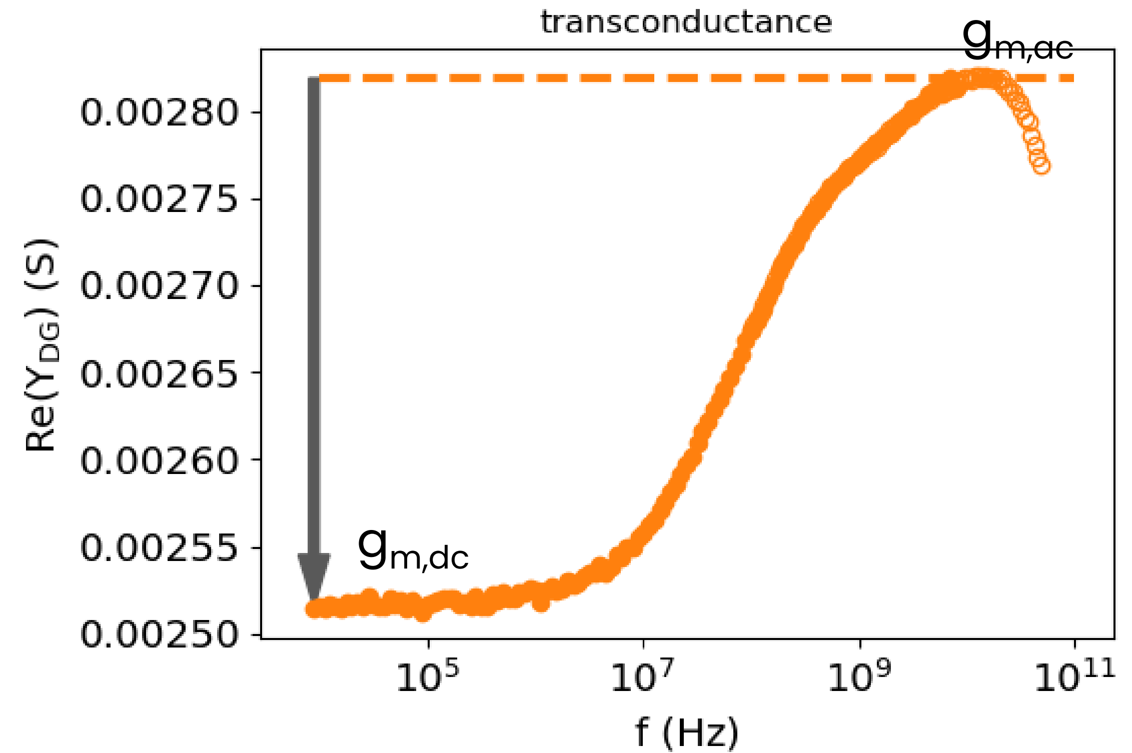
- transcapacitance *increases by orders-of-magnitude*

extracting the thermal resistance

extraction of the total thermal resistance





$$R_{\mathrm{th,g_{out}}} = \frac{g_{\mathrm{out,dc}} - g_{\mathrm{out,ac}}}{S_{\mathrm{I}} \cdot (I + V_{\mathrm{DS}} \cdot g_{\mathrm{out,ac}})}$$

$$R_{\mathrm{th,g_{m}}} = \frac{g_{\mathrm{m,dc}} - g_{\mathrm{m,ac}}}{S_{\mathrm{I}} \cdot V_{\mathrm{DS}} \cdot g_{\mathrm{m,ac}}}$$

$$S_{\mathrm{I}} = \frac{\mathrm{d}I_{\mathrm{D}}}{\mathrm{d}T_{\mathrm{amb}}}$$

extraction of the total thermal resistance: additional remarks (i)

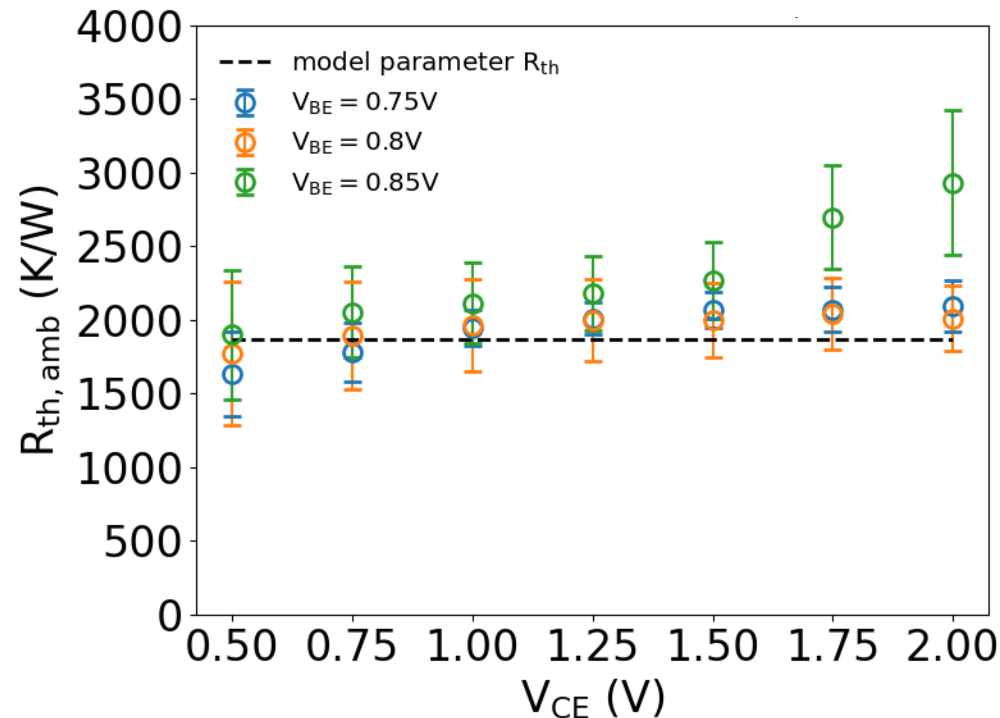
- method is 'exact' under the assumptions that
  - device is characterized by a single, 'lumped', ΔT
    → temperature gradients across device are not accounted for
  - for device without SH, output conductance and transconductance are frequency independent
  - thermal resistance is independent of temperature
- with a compact model one can easily verify this, by applying extraction methodology on simulated curves
- PSP example:

R_{th} model parameter	10000
R_{th} extracted from g_{out}	10000.095
R_{th} extracted from g_m	10000.095

- AC conductance method gives almost perfect result!
- accuracy limited by finite T-step in dI_D/dT_{amb} determination (small-signal quantity)
- confirms that there are *no* mathematical approximations

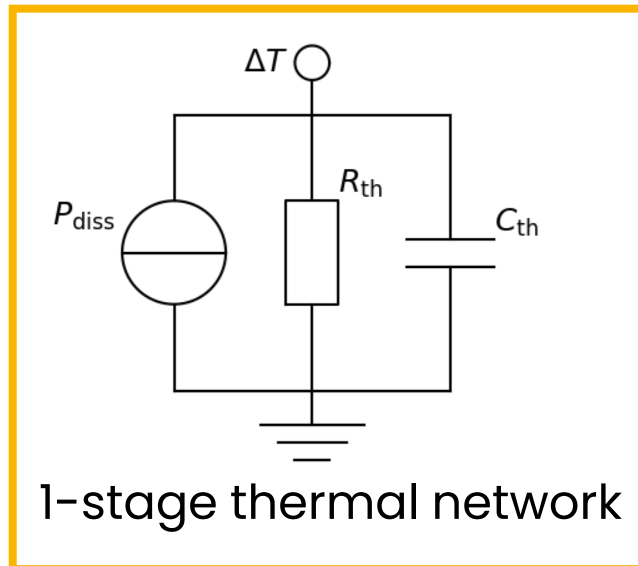
extraction of the total thermal resistance: additional remarks (ii)

- good practice to extract R_{th} from both output conductance and transconductance
- theoretically, these should give exactly the same results
- in practice, this is not the case, mainly due to parasitic-resistance effects, kicking in at high frequencies
- extracting R_{th} from in both ways this can be used to get a feeling for accuracy of R_{th} determination

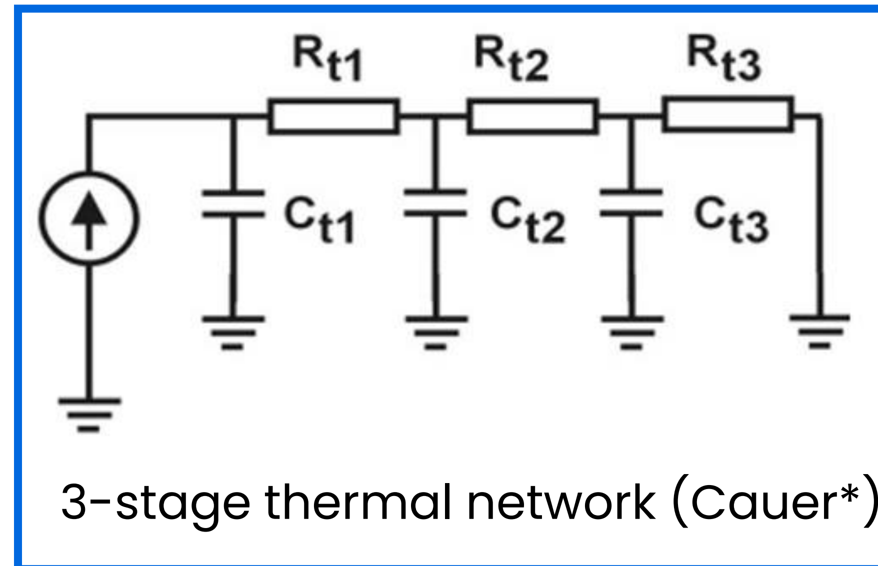


extraction of the total thermal resistance: additional remarks (iii)

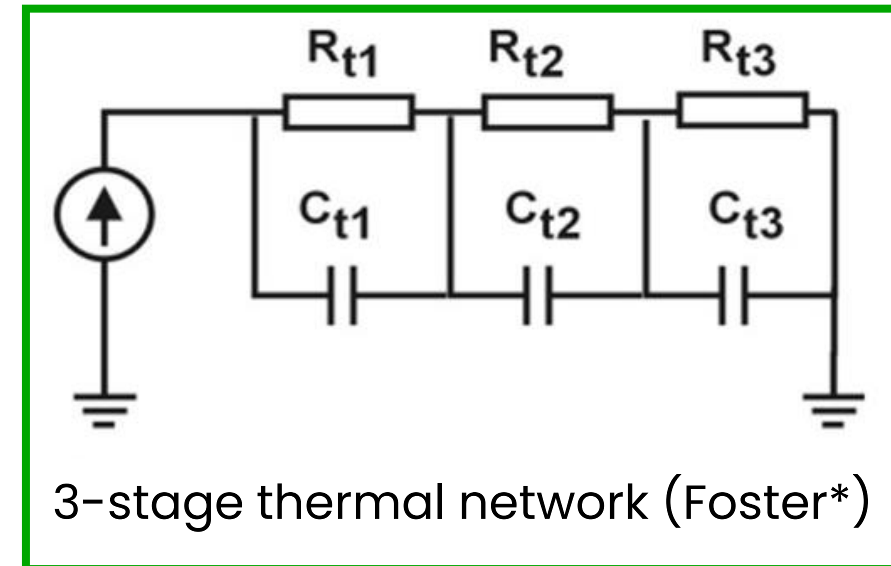
- method can also be used to extract thermal network, i.e. multi-stage network of resistors and capacitors describing the heating/cooling of the device
- in this talk, we mainly focus on
  - single-stage network description
  - total thermal resistance, i.e. DC resistance between ΔT and ground



1-stage thermal network



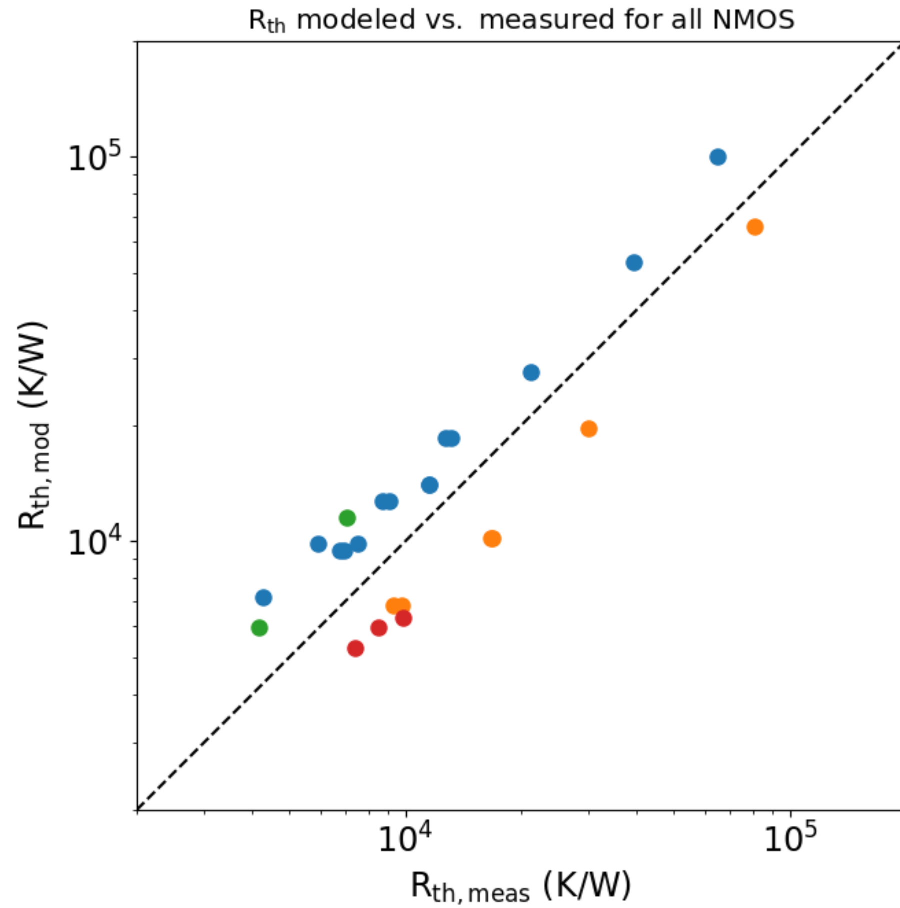
3-stage thermal network (Cauer*)

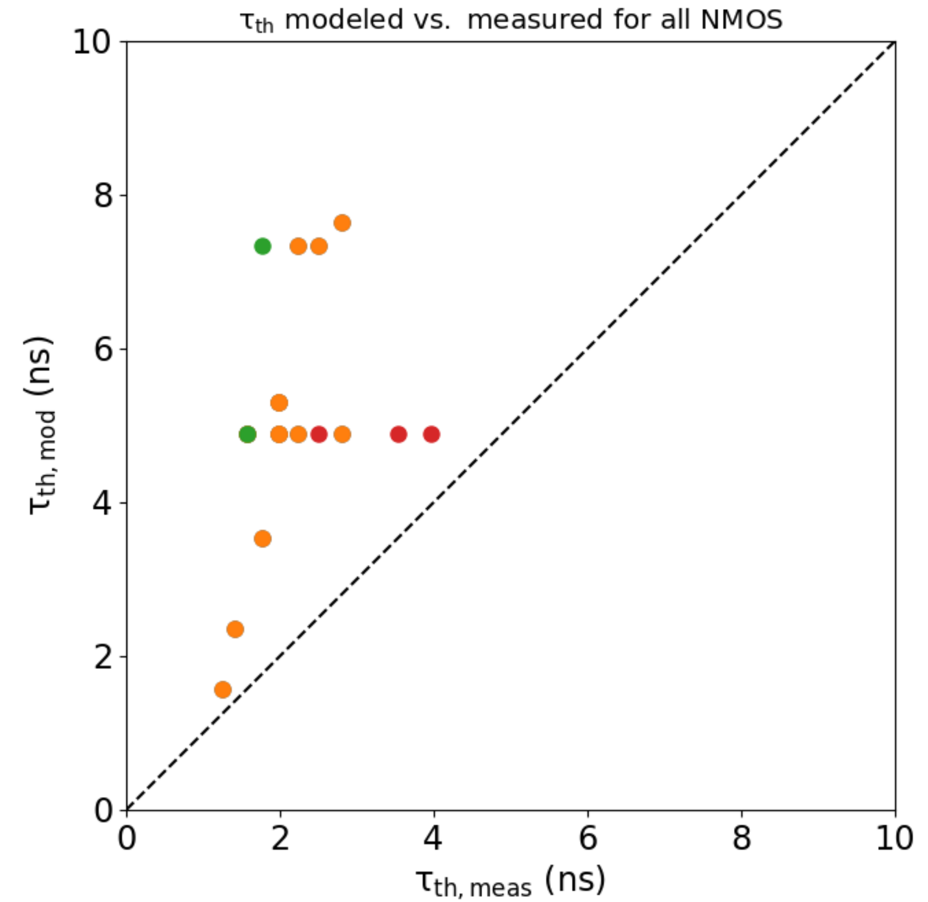


3-stage thermal network (Foster*)

*K.V.V.Murthy and R.E. Bedford, *Transformation Between Foster and Cauer Equivalent Networks*, IEEE Transactions on Circuits and Systems, Vol. 25, No. 4, pp. 238–239 (1978).

some results (FDSOI)





reasonable agreement between our measurements and foundry model

concluding remarks

AC conductance method pros and cons

- advantages
  - relatively simple
  - assesses static self-heating (R_{th}) as well as dynamic self-heating (C_{th})
  - mathematically 'exact' within the stated assumptions
  - gives parameters that directly apply to compact model implementations (single ΔT)
  - can be applied to great variety of devices
- limitations
  - difficult to make it very accurate
    - low-frequency limit not always achieved, and specific measurement difficulties
    - high-frequency limit can be blurred by parasitic resistance effects
    - dI/dT measurement needs to be in small-signal limit (i.e., small ΔT): not as easy as it seems
  - not suitable when devices exhibit strong trapping effects